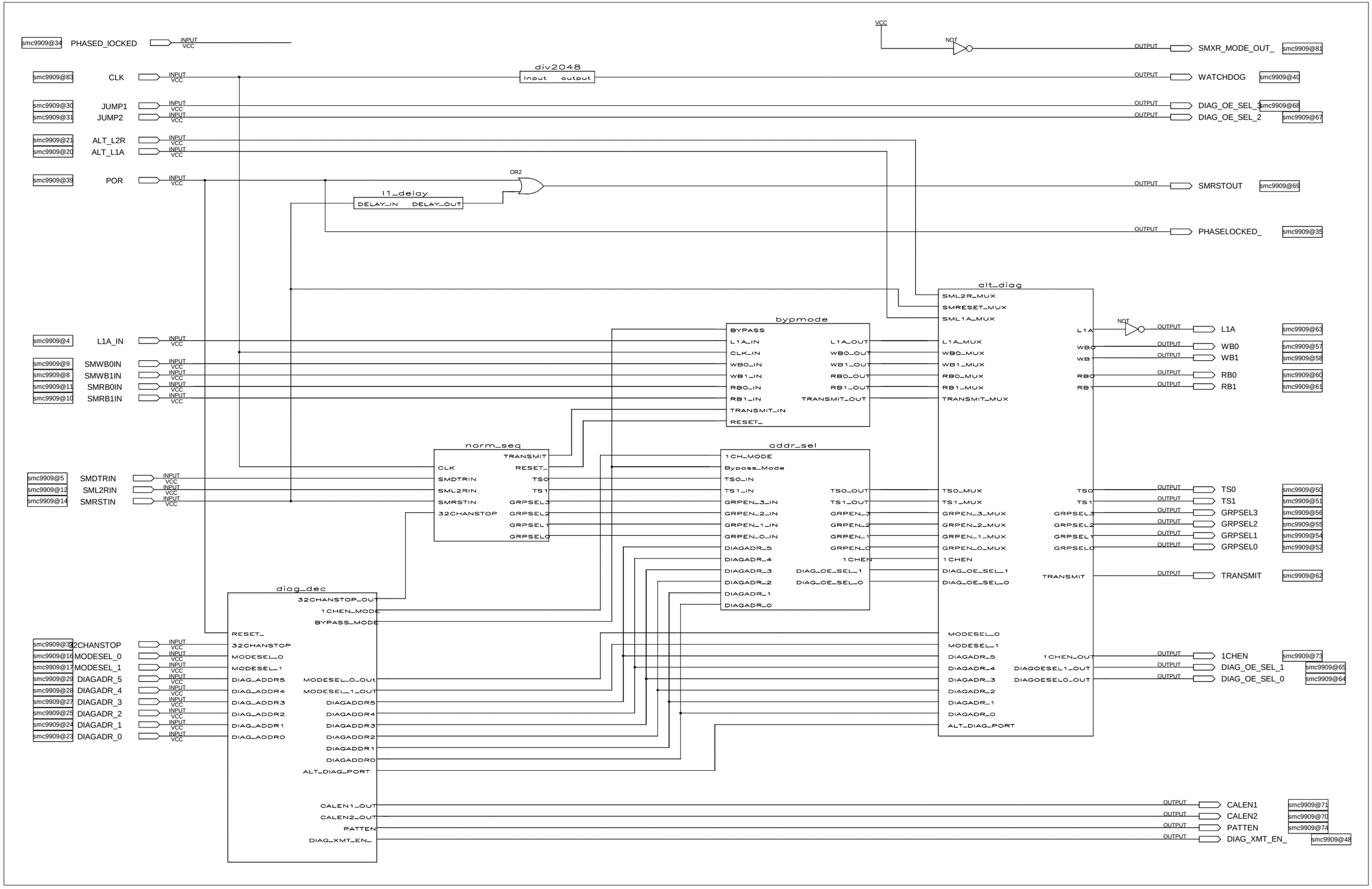
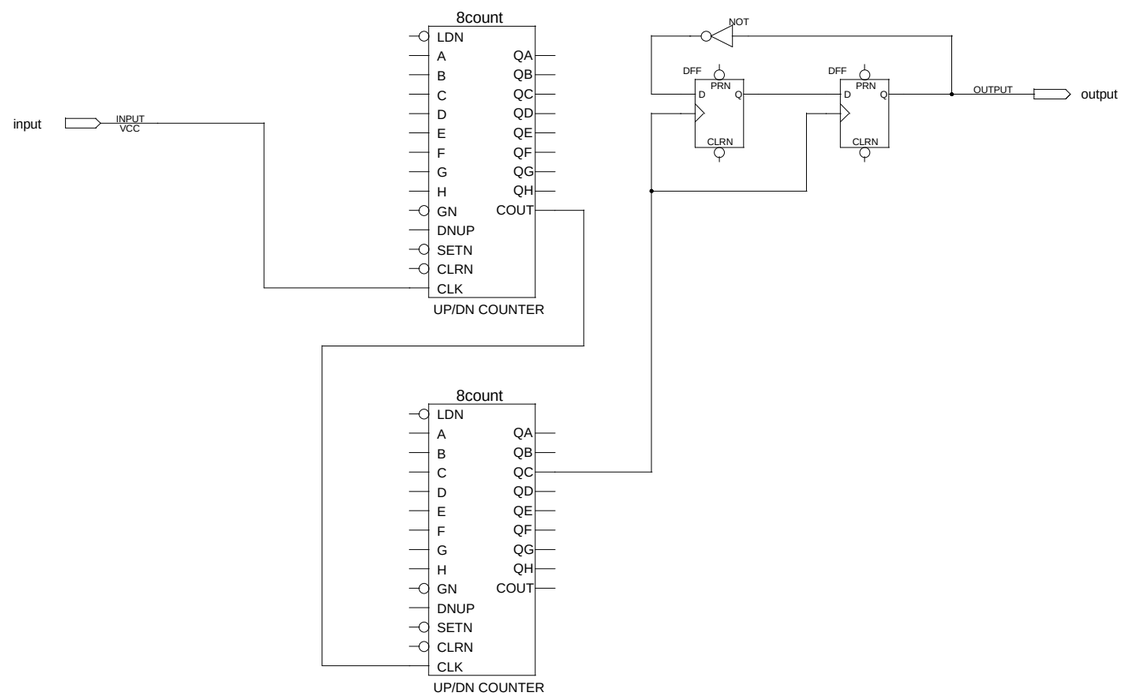
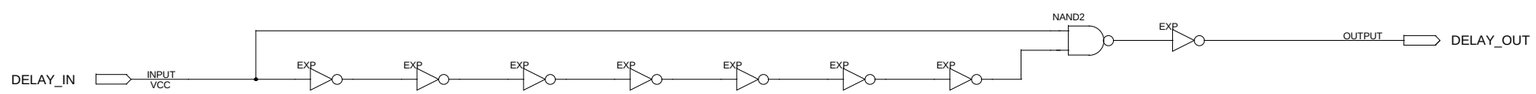
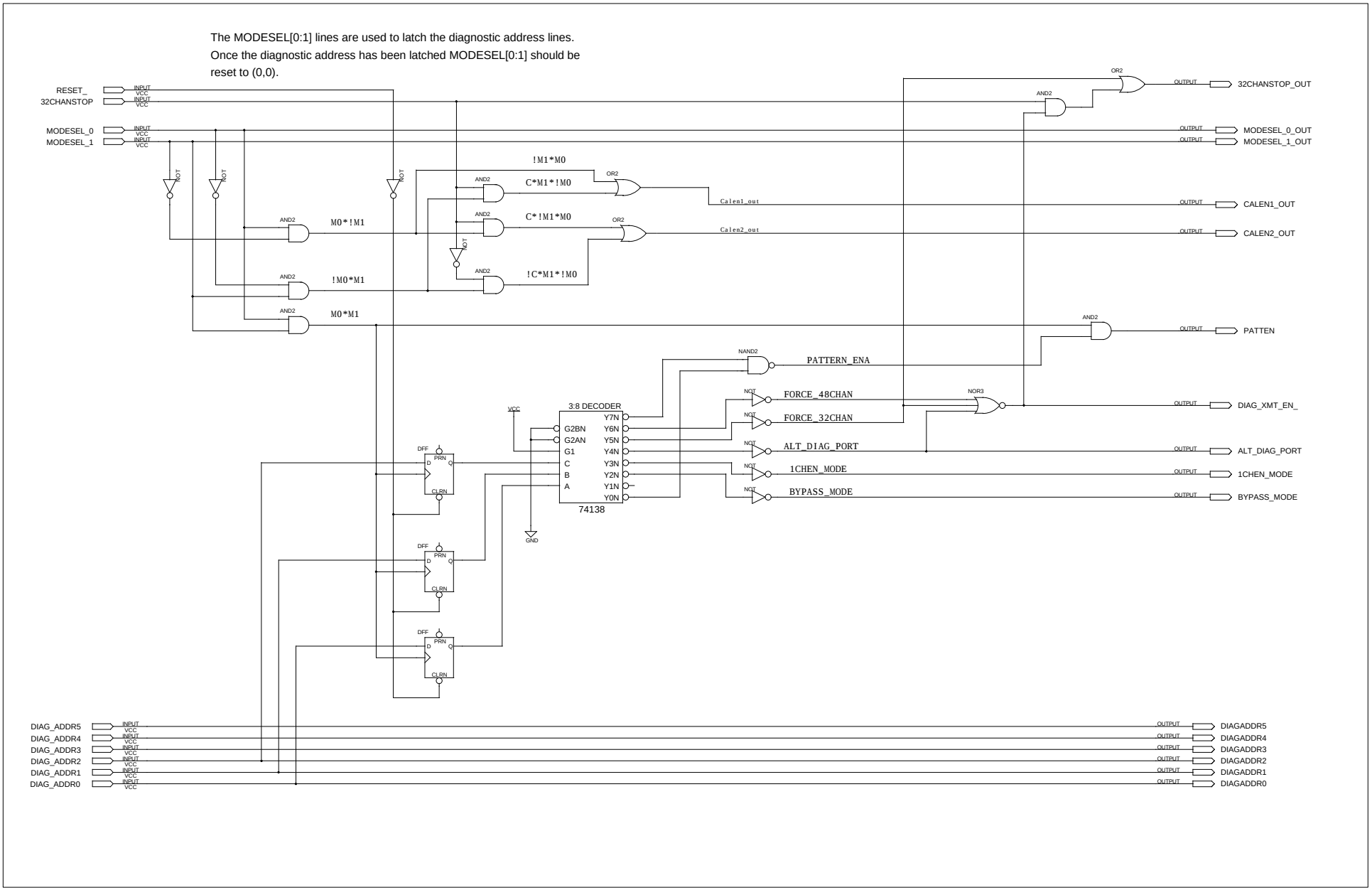
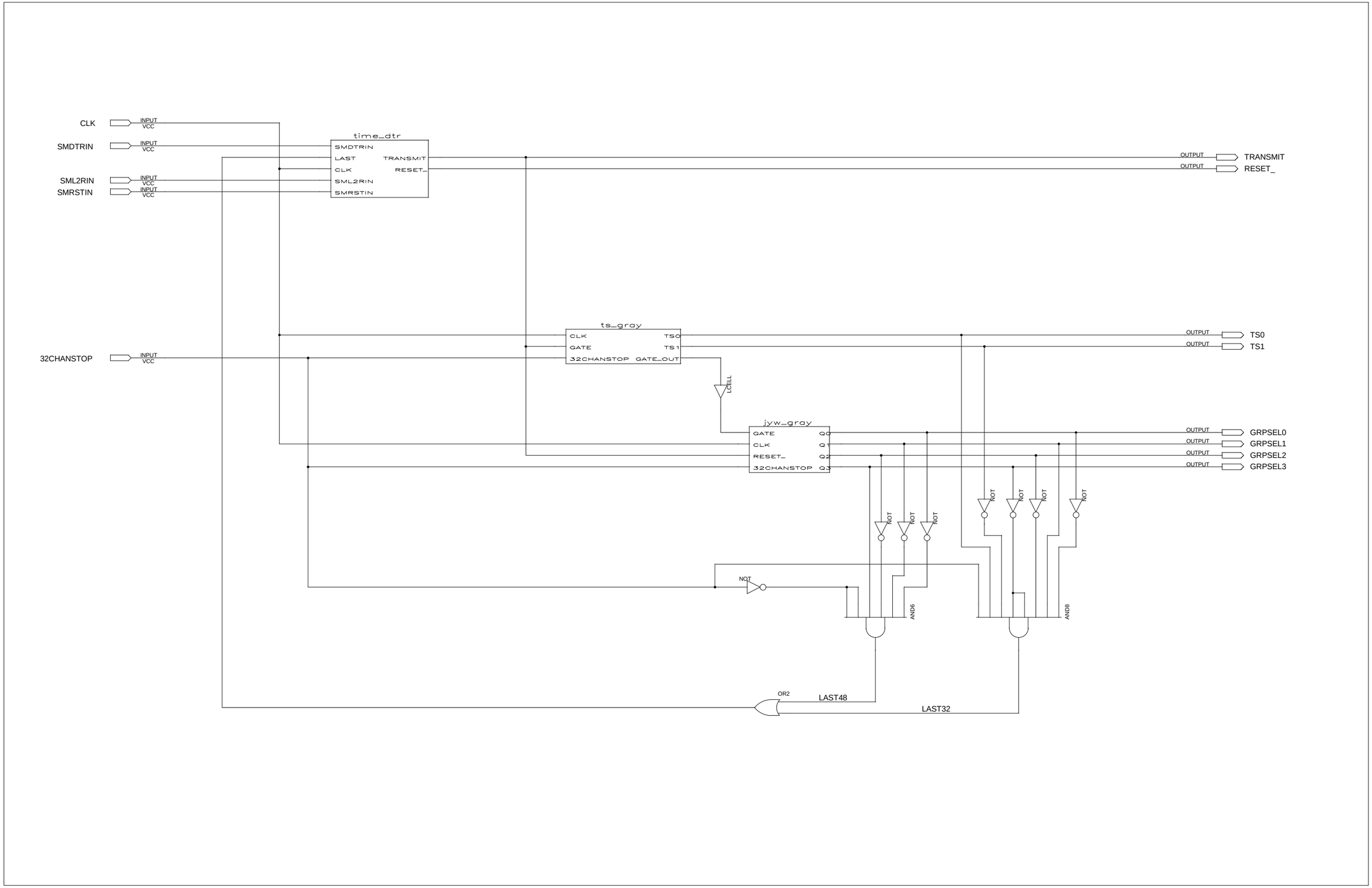
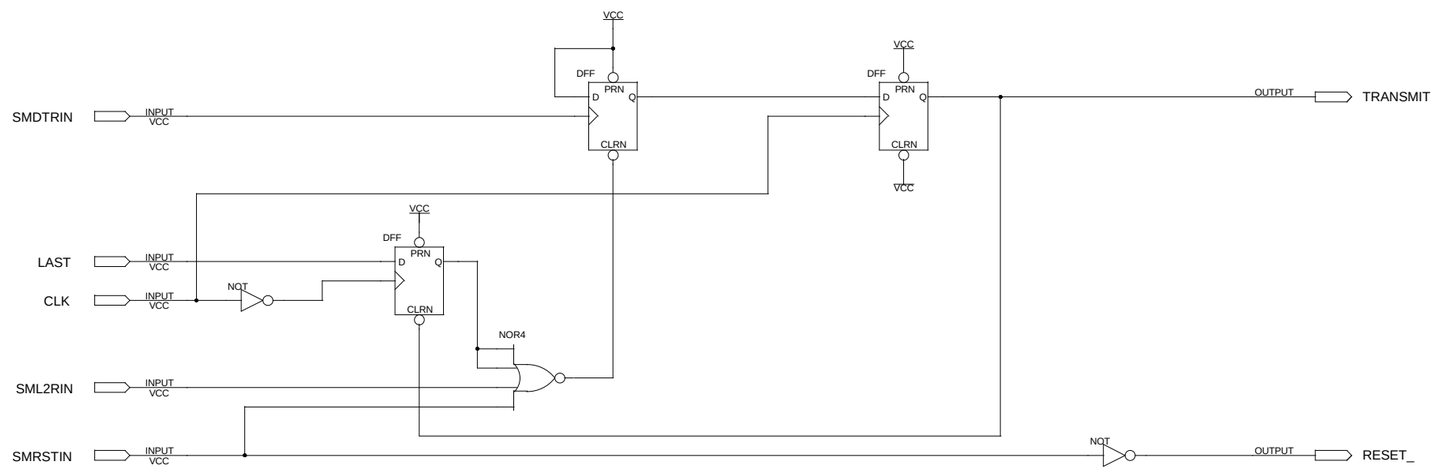

smc9909@34 PHASED_IOCKED
INPUT VCC
VCC
NOT
OUTPUT
SMXR_MODE_OUT_ smc9909@81
smc9909@83 CLK
div2048
input output
WATCHDOG smc9909@40
smc9909@30 JUMP1
smc9909@31 JUMP2
DIAG_OE_SEL_3 smc9909@68
DIAG_OE_SEL_2 smc9909@67
smc9909@21 ALT_L2R
smc9909@20 ALT_L1A
smc9909@39 POR
OR2
l1_delay
DELAY_IN DELAY_OUT
SMRSTOUT smc9909@69
PHASELOCKED_ smc9909@35
alt_diag
SML2R_MUX
SMRESET_MUX
SML1A_MUX
L1A_MUX
WB0_MUX
WB1_MUX
RB0_MUX
RB1_MUX
TRANSMIT_MUX
L1A
WB0
WB1
RB0
RB1
L1A smc9909@63
WB0 smc9909@57
WB1 smc9909@58
RB0 smc9909@60
RB1 smc9909@61
smc9909@4 L1A_IN
smc9909@9 SMWB0IN
smc9909@8 SMWB1IN
smc9909@11 SMRB0IN
smc9909@10 SMRB1IN
bypmode
BYPASS
L1A_IN
CLK_IN
WB0_IN
WB1_IN
RB0_IN
RB1_IN
TRANSMIT_IN
RESET_
L1A_OUT
WB0_OUT
WB1_OUT
RB0_OUT
RB1_OUT
TRANSMIT_OUT
norm_seq
CLK
SMDTRIN
SML2RIN
SMRSTIN
32CHANSTOP
TRANSMIT
RESET_
TS0
TS1
GRPSEL3
GRPSEL2
GRPSEL1
GRPSEL0
addr_sel
1CH_MODE
Bypass_Mode
TS0_IN
TS1_IN
GRPEN_3_IN
GRPEN_2_IN
GRPEN_1_IN
GRPEN_0_IN
DIAGADR_5
DIAGADR_4
DIAGADR_3
DIAGADR_2
DIAGADR_1
DIAGADR_0
TS0_OUT
TS1_OUT
GRPEN_3
GRPEN_2
GRPEN_1
GRPEN_0
1CHEN
DIAG_OE_SEL_1
DIAG_OE_SEL_0
TS0_MUX
TS1_MUX
GRPEN_3_MUX
GRPEN_2_MUX
GRPEN_1_MUX
GRPEN_0_MUX
1CHEN
DIAG_OE_SEL_1
DIAG_OE_SEL_0
TS0
TS1
GRPSEL3
GRPSEL2
GRPSEL1
GRPSEL0
TRANSMIT
TS0 smc9909@50
TS1 smc9909@51
GRPSEL3 smc9909@56
GRPSEL2 smc9909@55
GRPSEL1 smc9909@54
GRPSEL0 smc9909@52
TRANSMIT smc9909@62
smc9909@5 SMDTRIN
smc9909@12 SML2RIN
smc9909@14 SMRSTIN
diag_dec
32CHANSTOP_OUT
1CHEN_MODE
BYPASS_MODE
RESET_
32CHANSTOP
MODESEL_0
MODESEL_1
DIAG_ADDR5
DIAG_ADDR4
DIAG_ADDR3
DIAG_ADDR2
DIAG_ADDR1
DIAG_ADDR0
MODESEL_0_OUt
MODESEL_1_OUT
DIAGADDR5
DIAGADDR4
DIAGADDR3
DIAGADDR2
DIAGADDR1
DIAGADDR0
ALT_DIAG_PORT
CALEN1_OUT
CALEN2_OUT
PATTEN
DIAG_XMT_EN_
MODESEL_0
MODESEL_1
DIAGADR_5
DIAGADR_4
DIAGADR_3
DIAGADR_2
DIAGADR_1
DIAGADR_0
ALT_DIAG_PORT
1CHEN_OUT
DIAGOESEL1_OUT
DIAGOESEL0_OUT
1CHEN smc9909@73
DIAG_OE_SEL_1 smc9909@65
DIAG_OE_SEL_0 smc9909@64
smc9909@32 32CHANSTOP
smc9909@16 MODESEL_0
smc9909@17 MODESEL_1
smc9909@29 DIAGADR_5
smc9909@28 DIAGADR_4
smc9909@27 DIAGADR_3
smc9909@25 DIAGADR_2
smc9909@24 DIAGADR_1
smc9909@23 DIAGADR_0
CALEN1 smc9909@71
CALEN2 smc9909@70
PATTEN smc9909@74
DIAG_XMT_EN_ smc9909@48


8count
LDN
A
B
C
D
E
F
G
H
GN
DNUP
SETN
CLRN
CLK
QA
QB
QC
QD
QE
QF
QG
QH
COUT
UP/DN COUNTER
input
INPUT
VCC
NOT
DFF
PRN
D
Q
CLRN
OUTPUT
output
8count
LDN
A
B
C
D
E
F
G
H
GN
DNUP
SETN
CLRN
CLK
QA
QB
QC
QD
QE
QF
QG
QH
COUT
UP/DN COUNTER

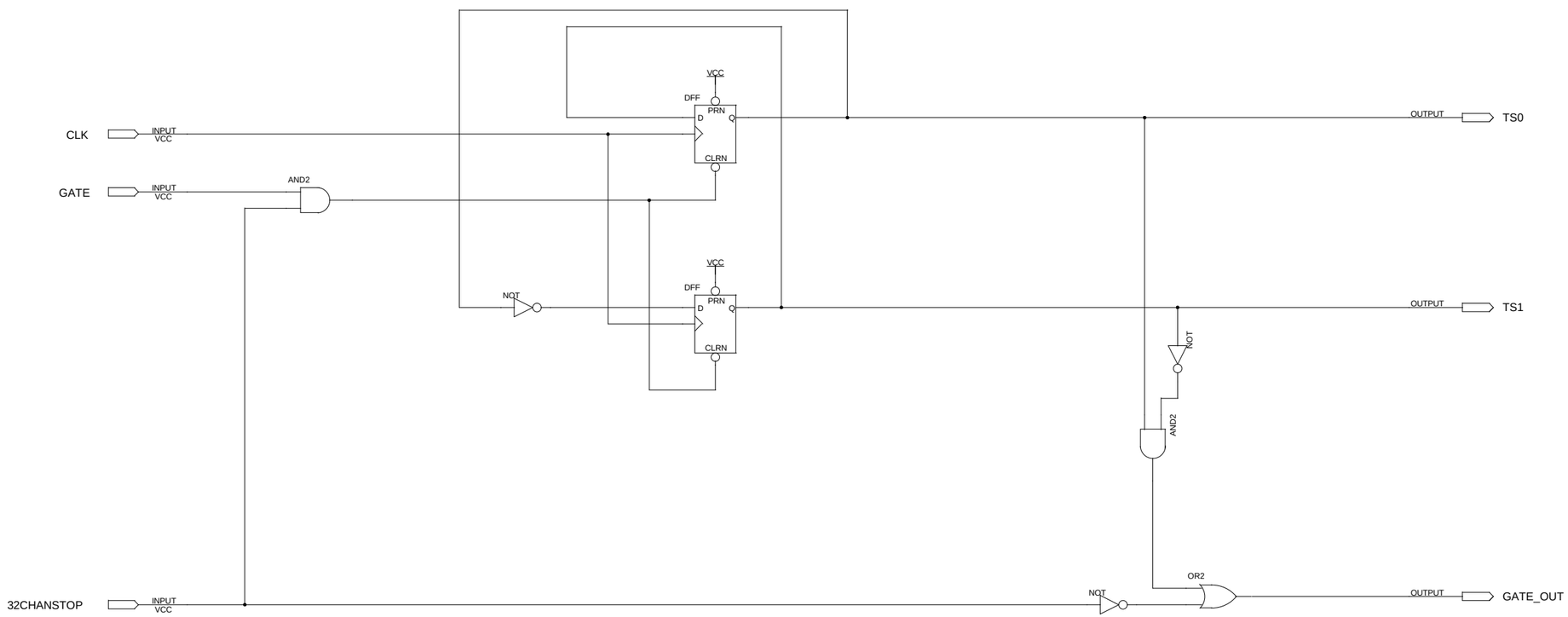

NAND2
EXP
OUTPUT
DELAY_OUT
DELAY_IN
INPUT
VCC
EXP
EXP
EXP
EXP
EXP
EXP
EXP

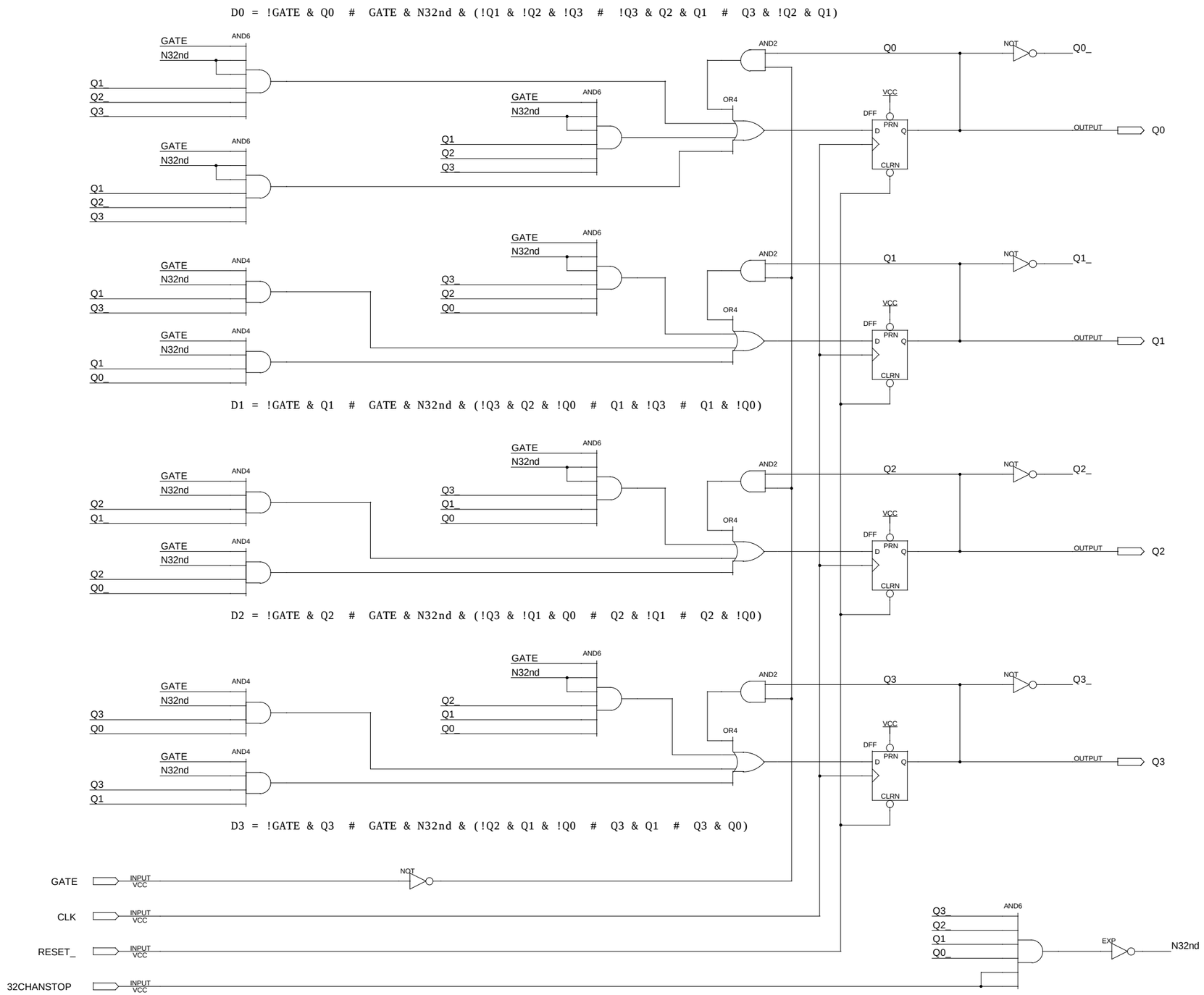

The MODESEL[0:1] lines are used to latch the diagnostic address lines.
Once the diagnostic address has been latched MODESEL[0:1] should be
reset to (0,0).
RESET_
32CHANSTOP
MODESEL_0
MODESEL_1
INPUT
VCC
NOT
AND2
OR2
M0*!M1
!M0*M1
M0*M1
!M1*M0
C*M1*!M0
C*!M1*M0
!C*M1*!M0
Calen1_out
Calen2_out
OUTPUT
32CHANSTOP_OUT
MODESEL_0_OUT
MODESEL_1_OUT
CALEN1_OUT
CALEN2_OUT
PATTEN
NAND2
PATTERN_ENA
FORCE_48CHAN
FORCE_32CHAN
ALT_DIAG_PORT
1CHEN_MODE
BYPASS_MODE
NOR3
DIAG_XMT_EN_
3:8 DECODER
G2BN
G2AN
G1
C
B
A
Y7N
Y6N
Y5N
Y4N
Y3N
Y2N
Y1N
Y0N
74138
GND
DFF
PRN
D
Q
CLRN
DIAG_ADDR5
DIAG_ADDR4
DIAG_ADDR3
DIAG_ADDR2
DIAG_ADDR1
DIAG_ADDR0
DIAGADDR5
DIAGADDR4
DIAGADDR3
DIAGADDR2
DIAGADDR1
DIAGADDR0


CLK
INPUT
VCC
SMDTRIN
SML2RIN
SMRSTIN
time_dtr
SMDTRIN
LAST
CLK
SML2RIN
SMRSTIN
TRANSMIT
RESET_
OUTPUT
TRANSMIT
RESET_
32CHANSTOP
ts_gray
CLK
GATE
32CHANSTOP
TS0
TS1
GATE_OUT
TS0
TS1
LCELL
jyw_gray
GATE
CLK
RESET_
32CHANSTOP
Q0
Q1
Q2
Q3
GRPSEL0
GRPSEL1
GRPSEL2
GRPSEL3
NOT
AND6
AND8
OR2
LAST48
LAST32


VCC
DFF
PRN
D
Q
CLRN
SMDTRIN
INPUT
VCC
OUTPUT
TRANSMIT
LAST
CLK
NOT
NOR4
SML2RIN
SMRSTIN
RESET_

| Inputs | Outputs TS0 | Outputs TS1 | Decimal Out |
|---|---|---|---|
| reset | 0 | 0 | 0 |
| clk | 0 | 1 | 2 |
| clk | 1 | 1 | 3 |
| clk | 1 | 0 | 1 |
| clk | 0 | 0 | 0 |



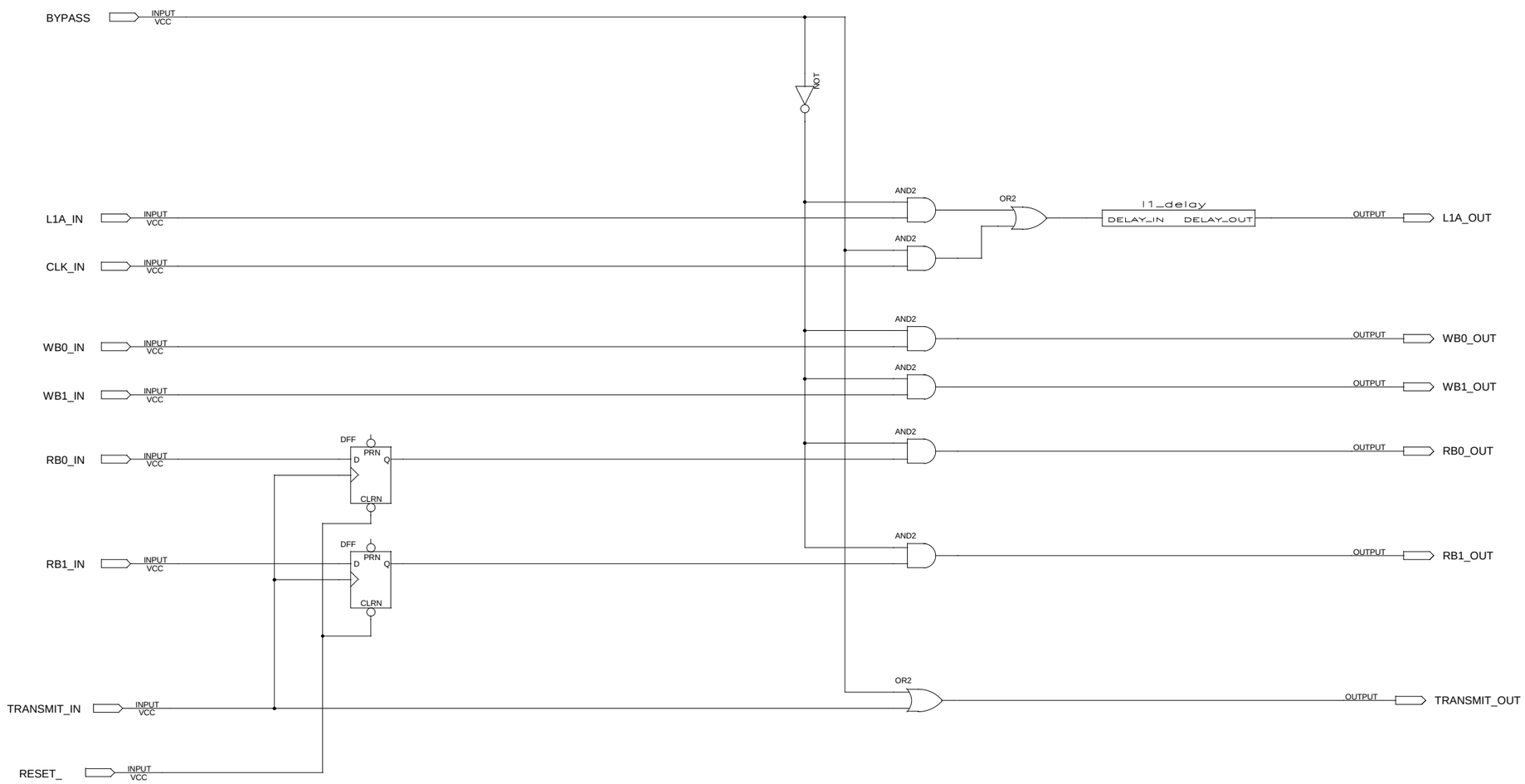


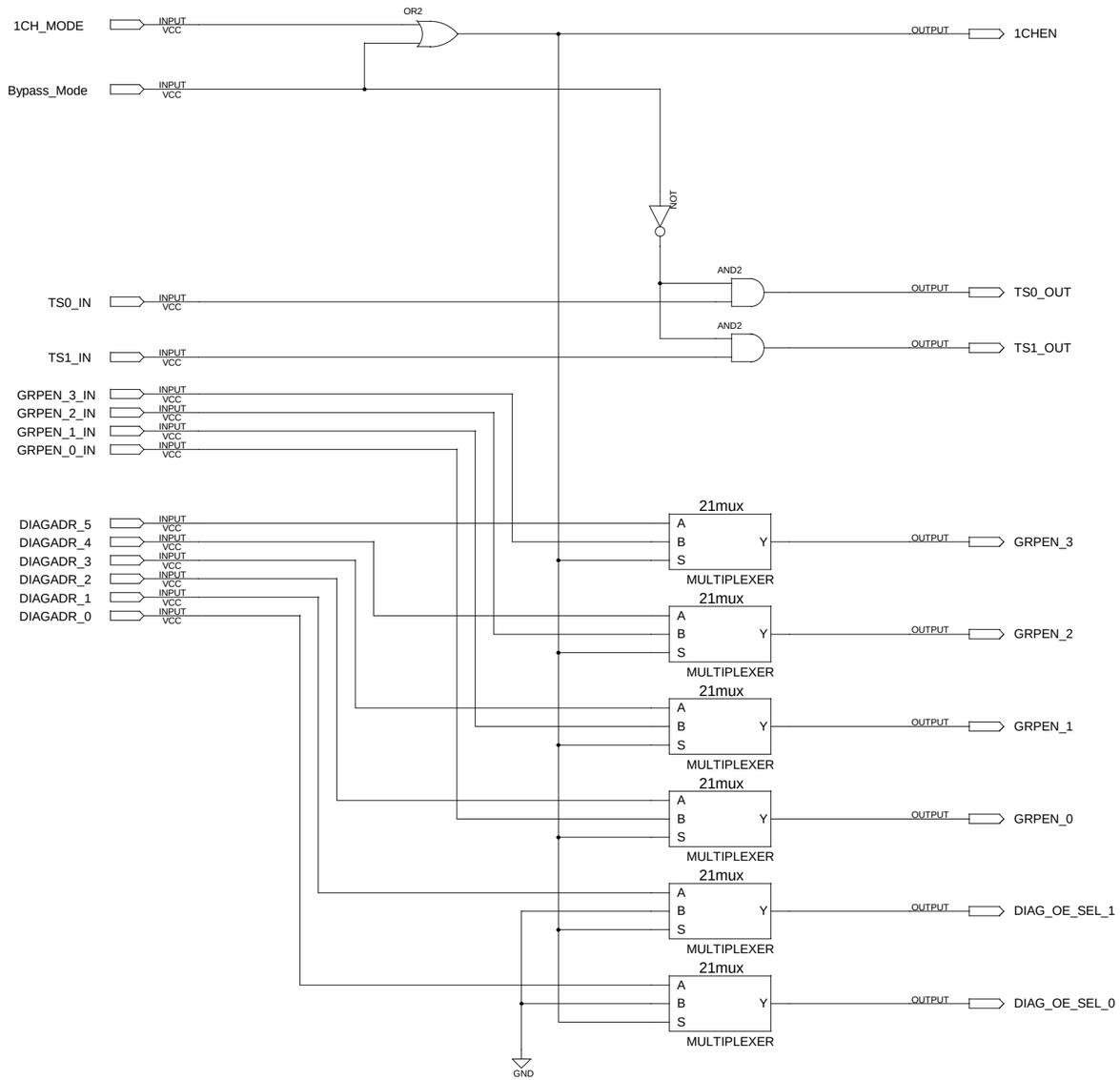

------if 32CHANSTOP = 0 ----

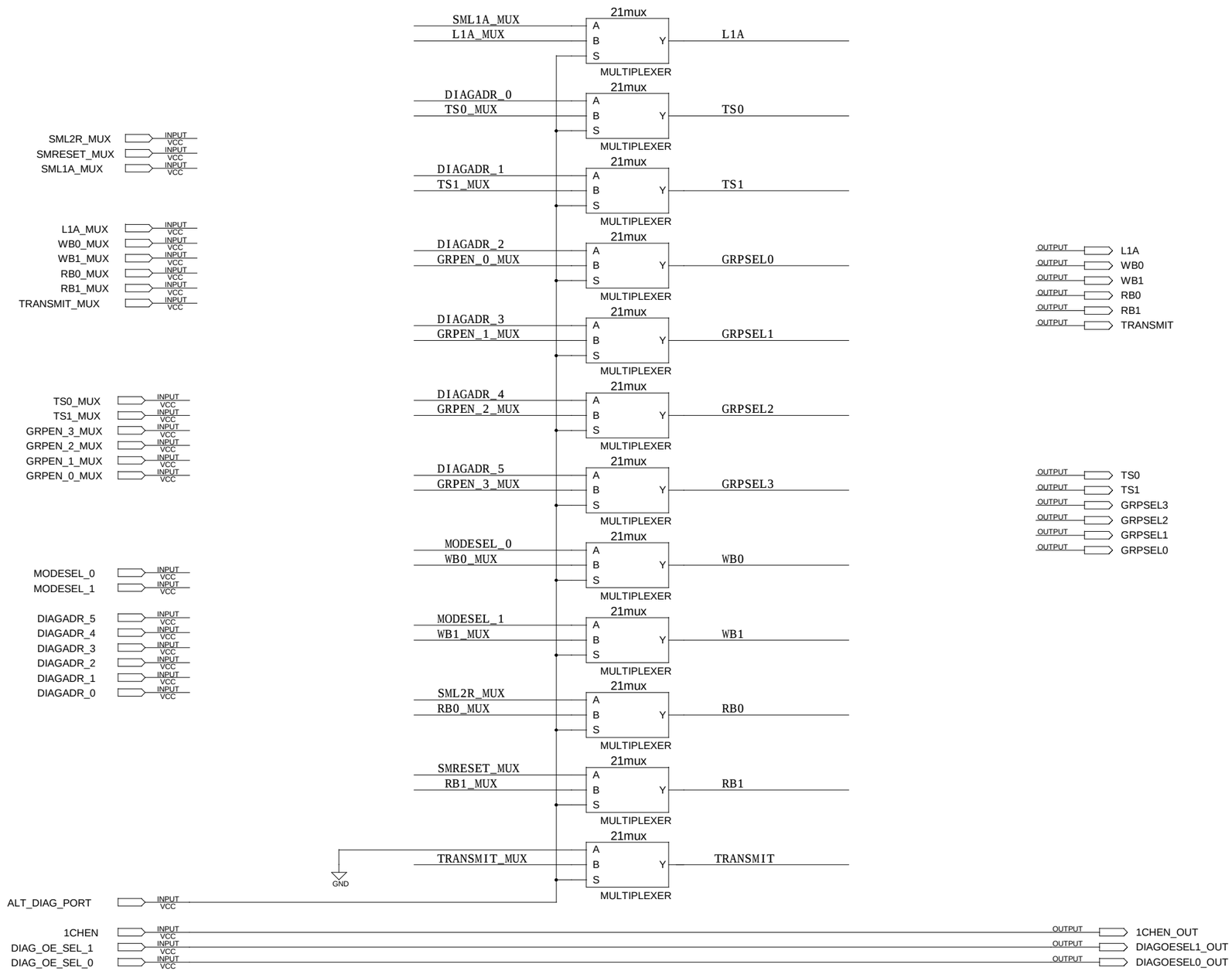
| After Input | Outputs Q0 | Q1 | Q2 | Q3 | Decimal Out |
|---|---|---|---|---|---|
| reset | 0 | 0 | 0 | 0 | 0 |
| clk | 1 | 0 | 0 | 0 | 1 |
| clk | 1 | 0 | 1 | 0 | 5 |
| clk | 0 | 0 | 1 | 0 | 4 |
| clk | 0 | 1 | 1 | 0 | 6 |
| clk | 1 | 1 | 1 | 0 | 7 |
| clk | 1 | 1 | 0 | 0 | 3 |
| clk | 0 | 1 | 0 | 0 | 2 |
| clk | 0 | 1 | 0 | 1 | 10 |
| clk | 1 | 1 | 0 | 1 | 11 |
| clk | 1 | 0 | 0 | 1 | 9 |
| clk | 0 | 0 | 0 | 1 | 8 |
| clk | 0 | 0 | 0 | 0 | 0 |

------if 32CHANSTOP = 1 ----

| After Input | Outputs Q0 | Q1 | Q2 | Q3 | Decimal Out |
|---|---|---|---|---|---|
| reset | 0 | 0 | 0 | 0 | 0 |
| clk | 1 | 0 | 0 | 0 | 1 |
| clk | 1 | 0 | 1 | 0 | 5 |
| clk | 0 | 0 | 1 | 0 | 4 |
| clk | 0 | 1 | 1 | 0 | 6 |
| clk | 1 | 1 | 1 | 0 | 7 |
| clk | 1 | 1 | 0 | 0 | 3 |
| clk | 0 | 1 | 0 | 0 | 2 |
| clk | 0 | 0 | 0 | 0 | 0 |


BYPASS
INPUT
VCC
NOT
L1A_IN
CLK_IN
WB0_IN
WB1_IN
RB0_IN
RB1_IN
TRANSMIT_IN
RESET_
AND2
OR2
l1_delay
DELAY_IN
DELAY_OUT
OUTPUT
L1A_OUT
WB0_OUT
WB1_OUT
RB0_OUT
RB1_OUT
TRANSMIT_OUT
DFF
PRN
D
Q
CLRN


1CH_MODE
INPUT
VCC
OR2
OUTPUT
1CHEN
Bypass_Mode
INPUT
VCC
NOT
AND2
TS0_IN
INPUT
VCC
OUTPUT
TS0_OUT
AND2
TS1_IN
INPUT
VCC
OUTPUT
TS1_OUT
GRPEN_3_IN
GRPEN_2_IN
GRPEN_1_IN
GRPEN_0_IN
DIAGADR_5
DIAGADR_4
DIAGADR_3
DIAGADR_2
DIAGADR_1
DIAGADR_0
21mux
A
B
S
Y
MULTIPLEXER
OUTPUT
GRPEN_3
GRPEN_2
GRPEN_1
GRPEN_0
DIAG_OE_SEL_1
DIAG_OE_SEL_0
GND


SML2R_MUX
SMRESET_MUX
SML1A_MUX
L1A_MUX
WB0_MUX
WB1_MUX
RB0_MUX
RB1_MUX
TRANSMIT_MUX
TS0_MUX
TS1_MUX
GRPEN_3_MUX
GRPEN_2_MUX
GRPEN_1_MUX
GRPEN_0_MUX
MODESEL_0
MODESEL_1
DIAGADR_5
DIAGADR_4
DIAGADR_3
DIAGADR_2
DIAGADR_1
DIAGADR_0
ALT_DIAG_PORT
1CHEN
DIAG_OE_SEL_1
DIAG_OE_SEL_0
INPUT
VCC
GND
21mux
A
B
S
Y
MULTIPLEXER
SML1A_MUX
L1A_MUX
L1A
DIAGADR_0
TS0_MUX
TS0
DIAGADR_1
TS1_MUX
TS1
DIAGADR_2
GRPEN_0_MUX
GRPSEL0
DIAGADR_3
GRPEN_1_MUX
GRPSEL1
DIAGADR_4
GRPEN_2_MUX
GRPSEL2
DIAGADR_5
GRPEN_3_MUX
GRPSEL3
MODESEL_0
WB0_MUX
WB0
MODESEL_1
WB1_MUX
WB1
SML2R_MUX
RB0_MUX
RB0
SMRESET_MUX
RB1_MUX
RB1
TRANSMIT_MUX
TRANSMIT
OUTPUT
L1A
WB0
WB1
RB0
RB1
TRANSMIT
TS0
TS1
GRPSEL3
GRPSEL2
GRPSEL1
GRPSEL0
1CHEN_OUT
DIAGOESEL1_OUT
DIAGOESEL0_OUT