

**Conceptual Design  
of the  
VME Interface  
for the  
MINOS Near Detector**

**By**

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## 1. Introduction

The front end electronics for the MINOS Near Detector has two parts. The MINDER Crate is a 6U crate that is located close to the MUX Boxes. This crate contains the QIE Digitizers. When data is digitized, it is held in local memories on boards that reside in the crate. After a data acquisition sequence, data is transmitted from these memories to a board in that resides in a VME Readout Crate, which can be far from the MUX boxes. The VME readout board is called the MASTER Module. The description of the system components and the operation of the system is described in [1].

In each VME Readout Crate, there resides a VME Processor. After data is sent to the MASTER Module and processed, it is stored in a buffer pending readout by the processor. This note describes details of how the processor functions in this system. It serves as a guide in the development of both hardware and software for the system.

## 2. VME Interface and Operational Issues

### A. Description of the Readout Buffers

There are two readout buffers on each MASTER Module. While one buffer is active for writing new data acquired from the MINDER Crate, the other buffer is made available to the VME processor for reading data previously acquired. In general, both buffers can be read by the VME Processor at any time. During data acquisition however, the VME Processor reads only one of them at a time, with the other one used for acquiring new data. In this way, completed data records are presented to the VME Processor, reducing ambiguities that might result if there were only one buffer that was active for both reading and writing at the same time.

The VME Crate can contain a number of MASTER Modules, and the buffers all change state at the same time. Furthermore, the change in state of the readout buffers is synchronized across the entire readout system of the Near Detector so that all readout buffers in the system change state at the same time. The control of the buffers is described in the next section.

### B. Buffer Control, and the Formation of Time Blocks

The system collects fragments of data from the entire detector, grouped into intervals of time called Time Blocks. This is done so that the software trigger can process the data that it receives efficiently. The Time Blocks are formed by controlling the length of time that a particular buffer on each MASTER Module is active for writing.

The control of the readout buffers is implemented by a special timing module that resides in the VME Crate, called the VME Timing Module (VTM.) This module receives a programmable Time Block Marker signal from the Master Clock System in the Near Detector, and uses it to generate VME Interrupts. The Interrupts are sent across the backplane of the VME crate. The MASTER Modules in the crate "spy" on the Interrupt signals, and use them to change state of the buffers. The VME Processor also receives the Interrupts, and uses them to initiate a new cycle for reading data from the buffers.

There are two readout buffers on each MASTER Module, and they may be located at different logical VME addresses. It is desirable for the buffer state to be synchronized across the entire crate, so that the VME Processor knows where in address space to read the data for a given Time Block period. To achieve this, the VTM uses two VME Interrupt signals, one for each buffer. (The selection of which of the VME Interrupts to use has not yet been made.) Each Interrupt will be asserted in alternating fashion, for example: first Interrupt A, then Interrupt B, then Interrupt A, etc. In this way, a particular readout buffer, along with its VME address space, is associated with a particular Interrupt signal. The convention shall be that the assertion of a particular Interrupt signal causes the associated buffer to be put into the "Read" state, with the other buffer put into the "Write" state. Each MASTER Module handles the control of its own buffers based on this convention.

The Time Block Marker signal from the Master Clock is programmable at the system level. It is a periodic signal, except for a special consideration described below. The nominal period is expected to be approximately 50 mS, with a range of 1 mS to 255 mS, in 1 mS steps (8 bits.) This is used to form Time Blocks of data across the entire system.

The Time Block Marker signal is fanned out to all VME Crates in the system simultaneously, so that readout buffers on MASTER Modules change state at the same time. Due to propagation delays, there may be an uncertainty in exactly when a buffer changes state on a given MASTER Module. The uncertainty is on the order of 200 nS across the entire system. The buffers do not change state in such a way as to cause data from a spill to be split between buffers (see below), so this uncertainty affects only data from cosmic rays. The Trigger and DAQ shall ensure that there is sufficient overlap of data fragments at the edges of Time Blocks, so that the loss of efficiency in triggering due to edge effects is reduced.

### C. Special Considerations for Spill Data

It is desirable for the change in buffer state (one going from write to read, and the other going from read to write) not to occur such that the data from a spill is split between buffers. The Master Clock System for the Near Detector is designed to prevent the change in buffer state from occurring within a certain time interval around the spill. This hold-off time interval is programmable in the Master Clock, and will ensure that the data from a spill has been fully processed by the Master module before the buffer state is allowed to change. Due to the aperiodic nature of the spills, this may result in some Time Blocks being slightly longer or shorter than nominal. The additional hold-off time will be the amount of time necessary to read in the data from a spill. For Single-Turn Extraction, this is expected to be approximately 300  $\mu$ S. Thus, in the worst case where the Time Block Marker signal occurs just after the Start-of-Spill signal is received, the Time Block would be extended by approximately 300  $\mu$ S. If the nominal Time Block is 50 mS, this corresponds to an increase in the interval of time by 6%. Note that no Time Block can have data from more than one spill (assuming a maximum range of 256 mS), since the spills as presently planned will not occur more frequently than 1-2 seconds apart. If this worst-case scenario occurs, the Time Block that contains the spill data would be 300  $\mu$ S longer than nominal. The following Time Block would then be 300  $\mu$ S shorter than nominal. The Time Blocks that follow would then return to nominal length.

### D. Special Considerations for Other Data

Outside of the spill, events can occur at any time. They can include cosmic rays, background radiation, LED pulsing, or PMT dark noise. When any of these random events occur, the readout is initiated by the dynode trigger. It will take approximately 5  $\mu$ Sec for the data from an isolated event to be transferred from the MINDER Crate to the MASTER Module. If a Time Block Marker occurs while data transmission is in progress, the MASTER Module does several things: it holds off changing the buffer state until the input channel that is transferring data is finished; it sends a signal to the MINDER Crate, holding off all further transmissions of data until after the buffer has changed state. If there is an event pending on a MINDER board, then the transmission will be delayed until after buffer has changed state. The worst case delay in this situation is 5  $\mu$ Sec. The VME Processor must hold off beginning a readout cycle after receiving the Interrupt from a Time Block Marker by this amount of time, to ensure that any data transmissions that were in progress have been completed.

**E. Data Format**

Each QIE data word is called a timeslice, because it represents the integral of the charge signal over one clock period, or "slice" of time. As the timeslice data is received and processed by the MASTER Module, the pedestal is subtracted on a channel-by-channel basis. The result is then compared to a programmable digital threshold. Any timeslice data that is over threshold is written into the active readout buffer. Every timeslice that is saved contains the amplitude, the timestamp, a channel ID, and error codes. A total of 64 bits, or 8 bytes, is written into the buffer. The format is given below:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
H	ERR[2:0]		GA[4:0]				ICH		CH[4:0]				ADC Value ADC[15:0]																			
L	DT[2:0]		X	Timestamp TS[26:16] Hi Word												Timestamp TS[15:0] Lo Word																

- ERR[2:0] - Error Codes (To be defined)
- DT[2:0] - Data Type (Used for indicating spill, calibration, etc.)
- GA[4:0] - Geographical Address
- ICH[2:0] - MASTER Module Input Channel (8 total)
- CH[4:0] - MINDER Module Channel Number
- ADC[15:0] - 16-Bit ADC Word for One Timeslice
- TS[26:0] - 32-Bit Timestamp for One Timeslice
- X[1:0] - Reserved

**Table 1. Data Format**

## F. Readout Buffer Size

The following are estimates of the amount of data that might be produced under certain operating conditions that might be viewed as the worst case. The estimates will be used to determine the size of the readout buffers.

For the high intensity beam, simulations show that a spill will create approximately 220 events on the average, with a sigma of approximately 15 events [2]. In a 'reasonable' worst case, the number of events in a spill could be 3 sigma higher than the average, or 265 events. Simulations also show that each event creates signals in approximately 90 photodetector channels on the average, but the distribution has a long tail. In the worst case, up to 400 channels could be hit. The QIE clock structure also adds a contribution. Because the time of arrival of charge from the photodetectors can be out of phase with respect to the 53 MHz clock, events can spread charge over several timeslices. The simulations show that the average number of timeslices per channel per event is ~2. Thus, a worst case estimate of the amount of data generated during a spill is given as:

$$265 \text{ Events} * 400 \text{ Channels/Event} * 2 \text{ Timeslices/Channel} * 8 \text{ Bytes/Timeslice} = 1.7 \text{ MB}$$

It will be assumed that the events are spread evenly throughout the detector, and that each VME Crate receives an equal amount of data from a spill. If there are 8 VME Crates, in the system, and each has 12 MASTER Modules, then the average worst case amount of data per MASTER Module is:

$$1.7 \text{ MB} / (8 \text{ VME Crates} * 12 \text{ MASTER Modules/VME Crate}) = \sim 18 \text{ KB}$$

If the buffers are 8 bytes wide (each data word is 8 bytes), then this corresponds to:

$$18 \text{ KB} / 8 \text{ Bytes/Word} = 2.25 \text{ KWords}$$

In addition to the data from a spill, the next largest source of events is the photodetector dark noise. If each pixel has a worst case of 50 Hz of noise, then an estimate of the amount of data in 256 mS, the largest possible Time Block, is:

$$8 \text{ MINDERS/MASTER} * 16 \text{ Channels/MINDER} * 50 \text{ Events/Sec/Channel} * 8 \text{ Bytes/Event} * 256 \text{ mSec} = 13 \text{ KB}$$

Again, if the buffers are 8 bytes wide, then this corresponds to:

$$13 \text{ KB} / 8 \text{ Bytes/Word} = 1.6 \text{ KWords}$$

Combining these two sources of data, the anticipated worst case buffer size in a 256 mSec Time Block is estimated to be ~4 KWords, or ~32 KBytes.

The size of each of the two buffers on the Master Module shall therefore be a minimum of 4K Words deep, at 8 Bytes/Word, or 32 KB. This corresponds to 500 words per buffer per MASTER input channel, or 4KB.

### G. Block Transfers of Data

The MASTER Module supports block transfers of data. The VME64X Specification states that the maximum size of a block transfer is 256 8-byte words. The VME interface on the MASTER Module shall abide by this specification. If data blocks are larger than this, then multiple block transfer cycles must be performed.

When the readout buffers change state, the MASTER Module writes the number of bytes of data into a register. The VME Processor can read this register to determine how many bytes it will receive in the transfer of data.

### H. Control of the MASTER Module

The MASTER Module has several different modes in which it can operate. The modes are shown in the table below. The mode of operation is controlled by setting bits in the Status Register. The VME Processor must select a mode as part of the setup of the MASTER Module, before an operation begins. {The Status Register bits have not yet been defined.}

<u>Mode #</u>	<u>Name</u>	<u>Function</u>
0	Standby Mode	Idle State
1	Data Mode	Normal DAQ (Physics)
2	Calibration Mode	Perform Calibrations
3	Flash Mode	Save/Recall Look-Up Tables
4	VME Mode	Perform VME I/O
5	Diagnostic Data Mode	Process Programmable Normal Data
6	Diagnostic Calibration Mode	Process Programmable CAL Data
7	LUT Diagnostic Mode	Look-Up Table Diagnostics

**Table 2. MASTER Module Functional Modes**

### **I. Address Modes**

The MASTER Module shall support two addressing modes:

- a. A32/D64 for Block Transfers
- b. A32/D32 for Non-Privileged Single Word (32 bit) Transfers

### **J. Geographical Addressing**

It is expected that the VME Crate for MINOS will support hard-wired Geographical Addressing as described in the VME 64 Extensions. The MASTER Module will use the slot information as part of the data word format.

## **3. Bibliography**

- [1] G. Drake, J. Dawson, C. Nelson, "Overview of the Front End Electronics for the MINOS Near Detector," Version 1.35, Nov. 15, 1999.
- [2] G. Pearce, Private Communication.