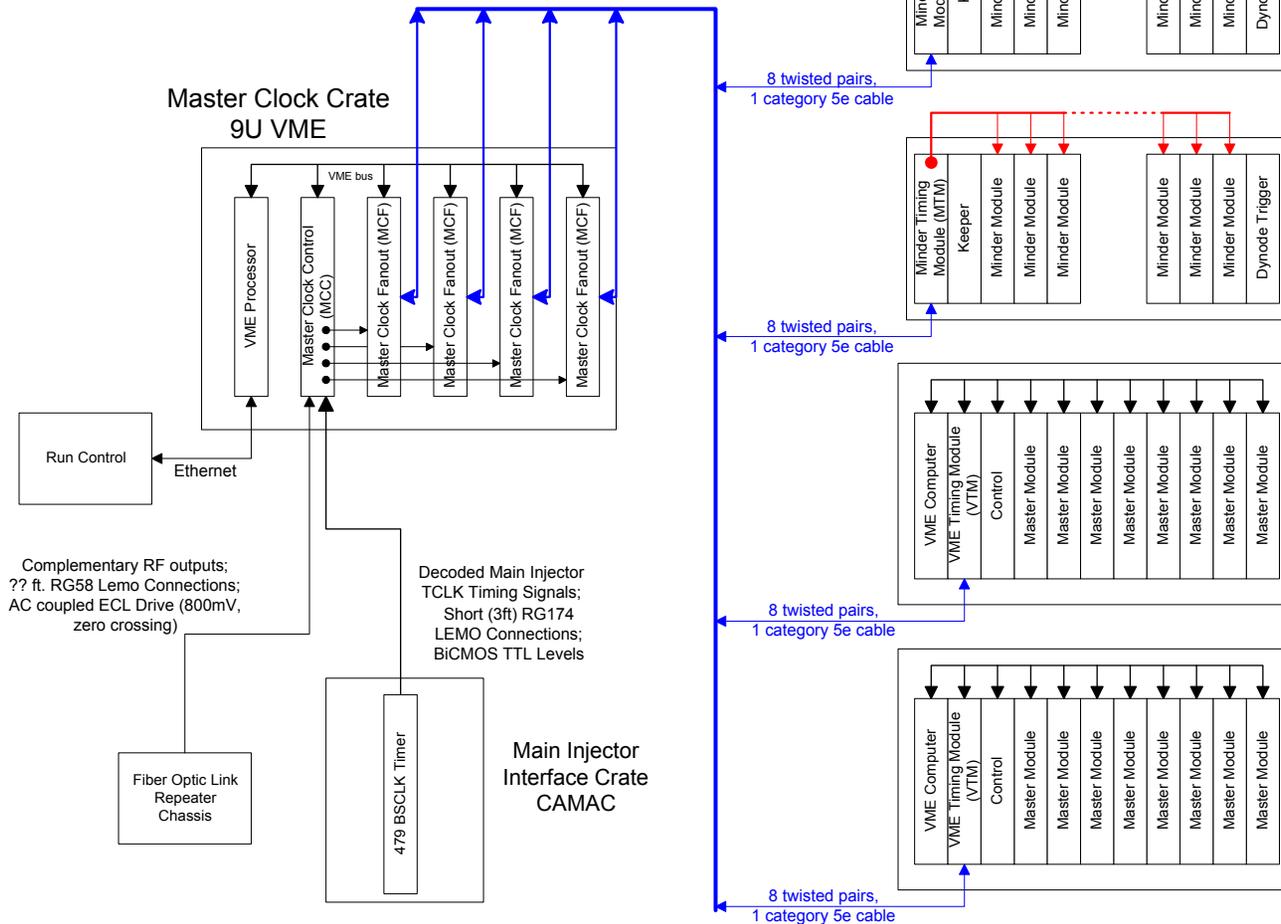


# MINOS Master Clock System Block Diagram

TJF 12/5/00

58 Serial Link Outputs (for Clock and control)  
and 58 slow control bi-directional connections to Front  
End Minder and VME Crates over single cable per crate;  
16 front panel RJ45 connectors per MCF module

Front Panel (point to point) Clock and Timing fanout from MTM  
16 Minder Modules via front panel RJ45 Jacks and Cat 5e/6cab

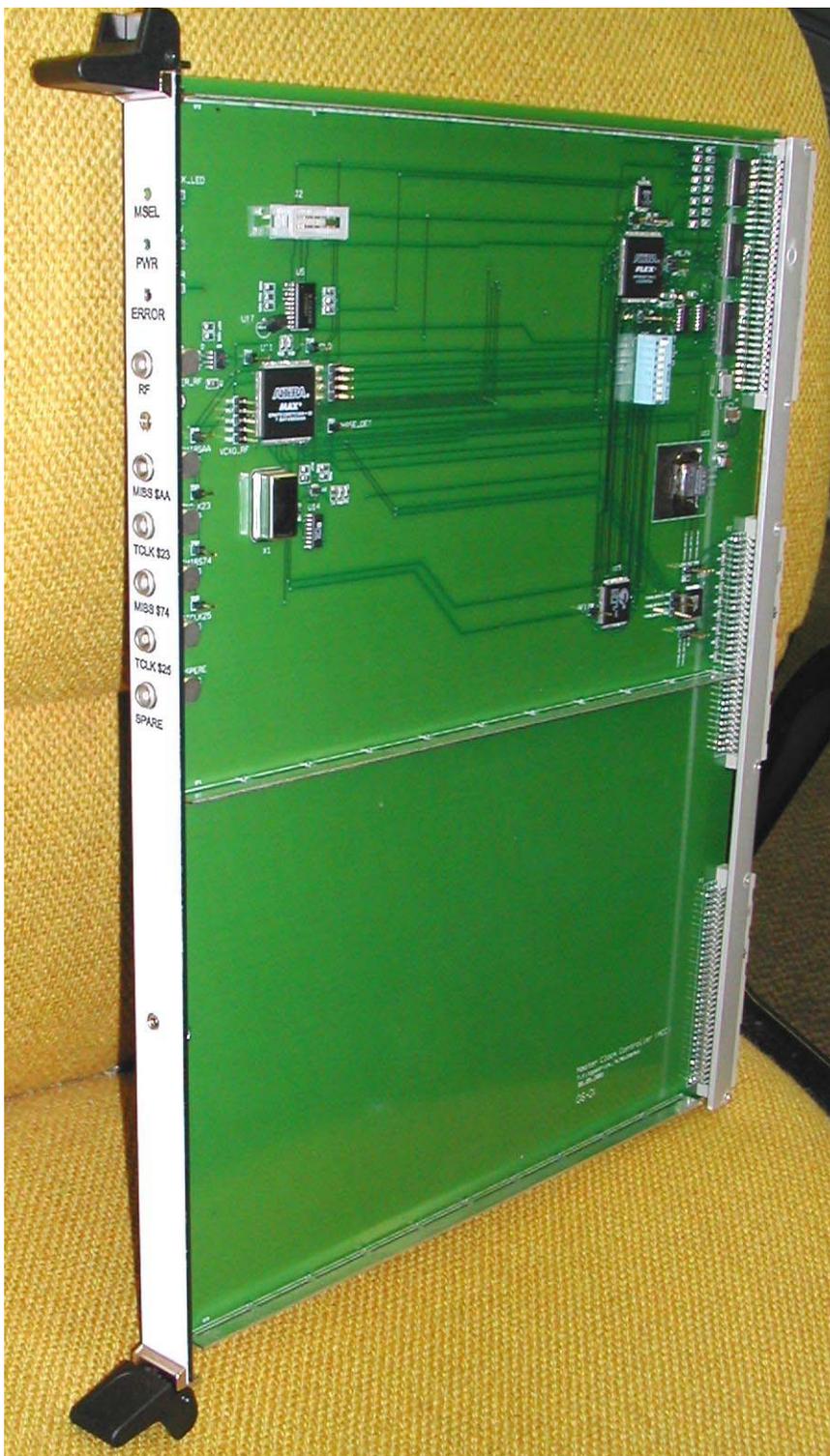


## CLOCK DESIGN FEATURES

- High speed serial link provides a fixed phase relationship between QCLK and timing signals to the front ends while still allowing QCLK phase adjustment.
- An LVDS-B serial slow control link is implemented for each front end connection to download delay information, monitor HOTLink lock status, initiate tests, etc.
- Clock, timing, and control connections provided using a single, low cost category 5 network-type cable for each front end.
- Master Clock Controller/Fanout configuration allows easy expansion of system.
- System runs with default parameters upon power up.

## MAIN FUNCTIONS OF MASTER CLOCK SYSTEM

1. Provides stable 53MHz clock (QCLK) for Front End Electronics at all times; locks onto Main Injector RF during Spill.
2. Provides programmable timing signals SGATE, CNTRST, TCAL, and TBMKR to front end electronics.
3. Provides global phase adjustment of QCLK relative to Main Injector RF in 24 steps of 785pS.
4. Provides individual QCLK fanout phase adjustment relative to Master Clock QCLK in 24 steps of 785pS.
5. Provides individual delay of front end timing signals relative to other front ends in 16 steps of 18.8nS.

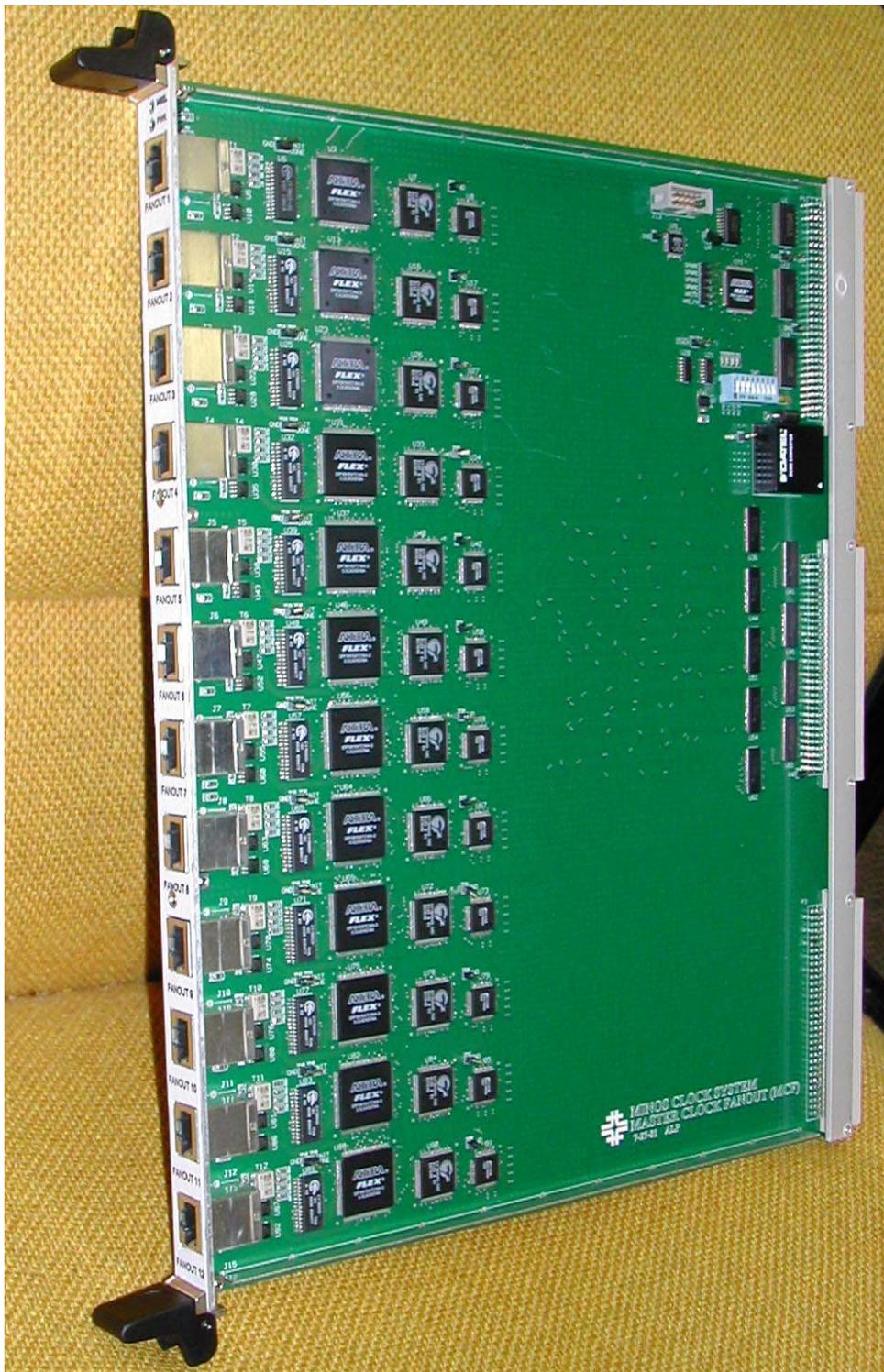


## MASTER CLOCK CONTROLLER (MCC)

- Main Injector Interface; receives Main Injector RF, receives and decodes various Tevatron and Main Injector marker signals, enabling MCC to detect a NuMI event and provide the appropriate timing signals to front end crates.
- VCXO based main oscillator allows MCC to lock on to Main Injector RF when it is stable during flat top, while also providing a stable QCLK to front end electronics during non-spill times.
- Generates all global clock and timing signals and fans them out on the backplane to the Master Clock Fanout cards (MCF).

### MCC VME Based User Interface

- Global phase of QCLK with respect to Beam can be adjusted in 24 steps of 785pS.
- Timing signals SGATE, CNTRST, TCAL, and TBMKR can be individually enabled or disabled. Each signal can also be “single pulsed” with a VME command.
- SGATE delay from kicker fire (MIBS \$74) programmable in 256 steps of 11.054uS (one Main Injector revolution) for a maximum delay of 2.83mS.
- SGATE duration programmable in 512 steps of 37.6nS for a maximum duration of 19.25uS.
- Local mode SGATE periodic programmable in 256 steps of 19.7mS for a maximum period of 5.04 seconds.
- CNTRST periodic programmable in 256 steps of 19.7mS for a maximum period of 5.04 seconds.
- TCAL periodic programmable in 64K steps of 154uS for a maximum period of 10 seconds.
- TBMKR periodic programmable in 512 steps of 616uS for a maximum period of 315mS

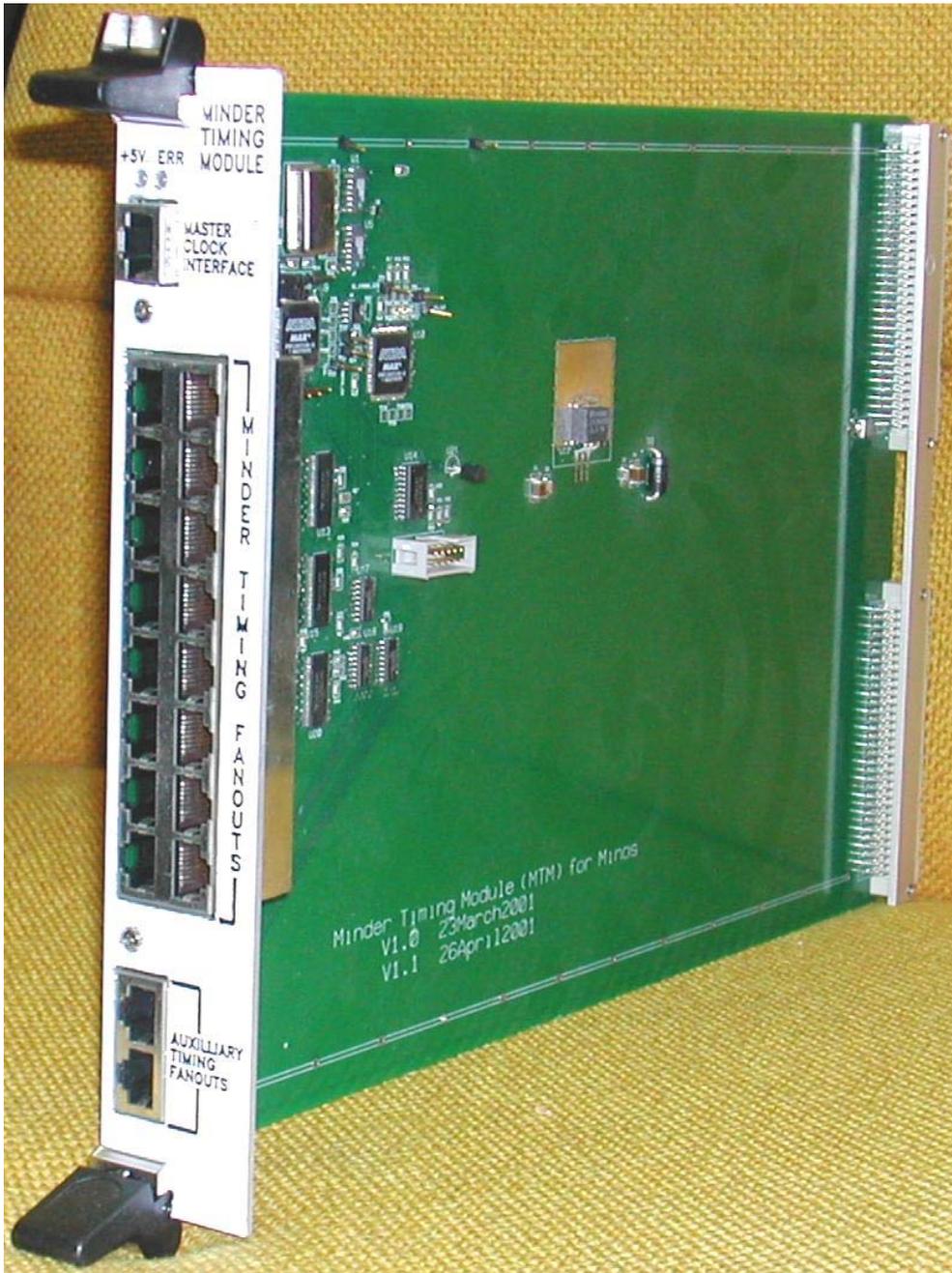


## MASTER CLOCK FANOUT (MCF)

- Receives QCLK and timing signals from MCC and provides up to 12 fanouts to front end Minder Timing Modules (MTM) or VME Timing Modules (VTM).
- Cypress HOTLink transmitters serialize timing signals with QCLK as the reference, ensuring that timing signals are properly phased to QCLK at the front end.
- Slow control serial interface using bi-directional LVDS allows communication between the Master Clock crate and individual front ends.

### MCF VME Based User Interface

- Phase of each fanout QCLK with respect to global QCLK can be adjusted in 24 steps of 785pS for a span of 18.8nS. This adjustment may be used for fine tuning of the QCLK with respect to beam for each front end crate.
- Each fanout provides coarse delay of three timing signals SGATE, CNTRST, and TCAL. The delay is programmed via the slow control interface in 16 steps of 18.8nS for a total delay of 300nS. This adjustment may be used to compensate for particle time of flight through the detector.
- MTM and VTM status read back via the slow control interface is provided for each of the 12 fanouts. The coarse timing signal delay settings can be read back, HOTLink tests can be initiated, and other latched status or errors are available.

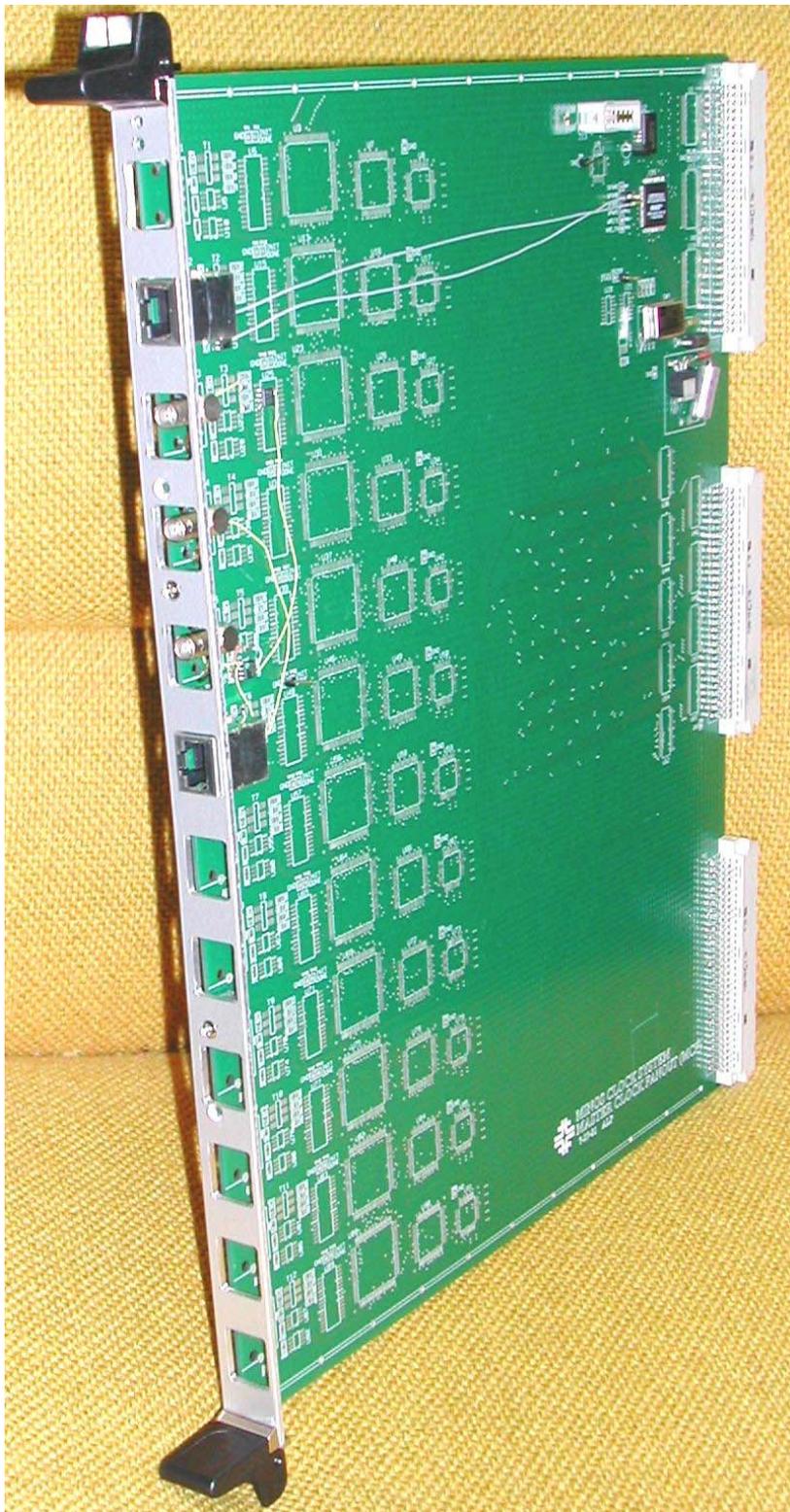


## MINDER TIMING MODULE (MTM)

- Cypress HOTLink receiver recovers QCLK and timing signals, which are fanned out to 16 parallel LVDS connections at the front of the module. QCLK variation between the 16 fanouts is less than 300pS.
- Slow control serial interface using bi-directional LVDS allows download of timing signal delay settings, read back of status, and other various test modes.

### MTM User Interface

- The MTM can be used without clock system by setting two on board jumpers to local mode. In this mode a QCLK and timing signals are provided with fixed periods.
- An error bit on the front panel of the MTM indicates loss of lock or data errors in the HOTLink transmitter/receiver circuitry. When the HOTLink connection is restored, the error disappears. The error bit also is driven out on J1 of the backplane.
- No power on setup is necessary for the MTM to produce QCLK and timing signals. Live insertion or extraction of any of the front panel cables will not harm the module.
- Although the Master Clock Interface connector is virtually identical to the 16 fanout connectors, the Master Clock Interface cable connector is keyed, reducing the possibility of incorrect connection.
- Two auxiliary fanouts are provided but the QCLKs are not as closely timed with the 16 main fanouts. (still within a few nanoseconds).



### **ND/FD Clock Interface for CALDET**

- An extra unstuffed MCF card was used as the form factor for the Near Detector/Far Detector Clock Interface board. This board resides in the Near Detector Master Clock Crate.
- Card receives LVDS driven 40MHz clock and Pulse Per Second (PPS) signals from the FD clock system via network type cable and RJ45 jack.
- Clock synthesizer chip produces a 53.1034MHz clock from the 40MHz clock ( $40\text{MHz} * 77/58$ ).
- Locally generated 40MHz clock and PPS signals are provided to test the interface board and MCC without the FD clock system. This output could conceivably be used as the FD Master Clock source as well.
- The two clocks and the PPS signal are passed along to the MCC via 3 front panel LEMO connectors.
- MCC VCXO locks to 53.1034MHz clock in the same way it would lock on to the Main Injector RF.

### **CALDET Operation of ND Clock System**

- The PPS signal is used to produce the CNTRST for the near detector front end electronics. Because the PPS is timed to the 40MHz FD clock, the ND CNTRST will have a phasing uncertainty of up to 36.5ns since CNTRST is clocked by  $QCLK/2$ . A 3.3V TTL level copy of CNTRST is provided on a LEMO connector at the front panel of the MCC should the CNTRST uncertainty between the two systems need to be resolved to a greater accuracy.
- TBMKR is also timed to PPS. To start a run, TBMKR is enabled through VME on the MCC. Logic within the MCC holds off the first TBMKR until the next PPS. TBMKR is then periodic synchronous to the 40MHz FD clock. TBMKR is also disabled on the PPS boundary, facilitating a smooth stop to a run.
- TBMKR is programmable to four periods in CALDET mode - 10mS, 25mS, 50mS, or 100mS.
- All stand alone functionality of the ND clock system is available by switching to local mode.
- Very little ND Clock setup is needed for CALDET. Simply turn the system power on and enable TBMKR to start a run. QCLK and timing signal phasing and delays are not thought to be useful for CALDET.

## ELECTRONICS REVIEW ISSUES

- **John Cobb states:**

The GPS time which is latched & stored should really be the time of the single turn extraction, rather than SGATE, which has to start 5 - 10 uSec ahead of the extraction to prepare the QIEs for spill data. At least the offset must be known and recorded somewhere. (Of course the neutrinos arrive at Soudan 2.433 mSec later).

Answer: The offset between SGATE and the actual time of the extraction will be constant to a resolution of one RF cycle. The actual number may not be determined until the clock system is running in the MINOS hall using Main Injector timing. Of course the length of the cables and phase/delay settings also affect the offset for each front end.

- **Bob Webb states:**

The timing of the clock system for the system requires cable runs be trimmed to 1 nsec. How many cables are there that need to be dealt with here?

Answer: There are about 60 cables at 100 feet each. The trimming of the cables is a desired feature so that a baseline timing is established for each front end. This is not a requirement of the clock system. The clock system will perform fine with any length cable up to about 200 feet.

## CLOCK SYSTEM STATUS

1. Three complete Master Clock Controller crates have been built and tested. A complete crate includes VME crate, backplane, power supply, prototype Master Clock Controller card, and prototype Master Clock Fanout card. Some small additions to the MCC will be necessary for production MINOS boards. No modifications have been identified for the MCF.
2. Ten Production Minder Timing Modules are built and tested. Unless problems are discovered with longer term testing, the MTM is also ready for full production.
3. A "Main Injector Emulator" board was built to test the MCC interface to the Main Injector. Further testing using real Main Injector hardware would be prudent to assure there are no surprises. So far the problem has been finding a suitable test area that has Tevatron encoded timing, Main Injector encoded timing, and RF repeater links available in the same area.
4. Diagnostic software to test various registers, memories, and the slow control interface of the MCC and MCF over longer periods with many loops is being developed.
5. Run control software integrating the clock system to the DAQ is being developed for CALDET that may be usable as a stepping stone to the MINOS run control software.