



Near Detector Electronics Tutorial
System Overview
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MINOS Near Detector Front End Electronics Tutorial

Overview of the System

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System Requirements

Operational Modes

- **Single-Turn Extraction Mode**
 - 10 uS Duration
 - ~1 Second Between Spills
 - Use Spill Signal from Accelerator for Trigger
 - Digitize and Record Data for Each RF Bucket
 - Store Data Locally Until After Spill



System Requirements

Operational Modes (Cont.)

• **Single-Turn Extraction Mode (Cont.)**

➤ Process Data After Spill

- Transmit Data to VME
- Zero-Suppress
- Form Timestamp
- Add Channel ID
- Store in Read-Out Buffer



System Requirements

Operational Modes (Cont.)

- **Cosmic Ray Mode**
 - Can Run Concurrently with Spill
 - Uses ~1 Second Duration Between Spills
 - Use Trigger from Dynode Discriminator
 - Digitize and Record 8 RF Clocks per Trigger



System Requirements

Operational Modes (Cont.)

- **Cosmic Ray Mode (Cont.)**
 - Process Data Promptly
 - Transmit Data to VME
 - Zero-Suppress
 - Form Timestamp
 - Add Channel ID
 - Store in Read-Out Buffer



System Requirements

Operational Modes (Cont.)

- **Resonant Extraction Mode**

- Tentative, Change to Firmware
- 1 mS Duration
- ~1 Second Between Spills
- Use Trigger from Dynode Discriminator
- Digitize and Record 8 RF Clocks per Trigger
- Store Data Locally Until After Spill



System Requirements

Operational Modes (Cont.)

• **Resonant Extraction Mode (Cont.)**

- Process Data After Spill
 - Transmit Data to VME
 - Zero-Suppress
 - Form Timestamp
 - Add Channel ID
 - Store in Read-Out Buffer



System Requirements

Performance Requirements

- **Least Count Resolution**

- Maximum PMT Gain of $1E6$
- Minimum Pixel Gain $\sim 1/3$ Lower
- 1 pe produces ~ 50 fC on Low Gain Pixel
- Target: $1sb = 7.5$ fc \rightarrow 2-3 fC



System Requirements

Performance Requirements (Cont.)

- **Largest Signal**

- Largest Signal ~ 25 mips
- ~ 6 pe/mip
- ~ 24 pC on Highest Gain Pixel

- **Dynamic Range**

- \rightarrow 12-13 Bits of Dynamic Range



System Requirements

Performance Requirements (Cont.)

- **Digitization Rate**

- Digitize at RF Clock Rate of 53 MHz

- **Deadtime**

- No Deadtime During STE

- ~80% Live Time for Cosmic Rays

- < 10 μ S Deadtime During Resonant Extraction



System Requirements

Performance Requirements (Cont.)

- **Timestamping**
 - Resolution of RF Clock (~ 19 nS)
- **Zero-Suppression**
 - All Events Zero-Suppressed before Readout



System Description

General Description

• 2 Primary Parts

➤ Front End Crate

- Analog Signal Processing and Digitization
- Temporary Data Storage
- Timestamp Counters

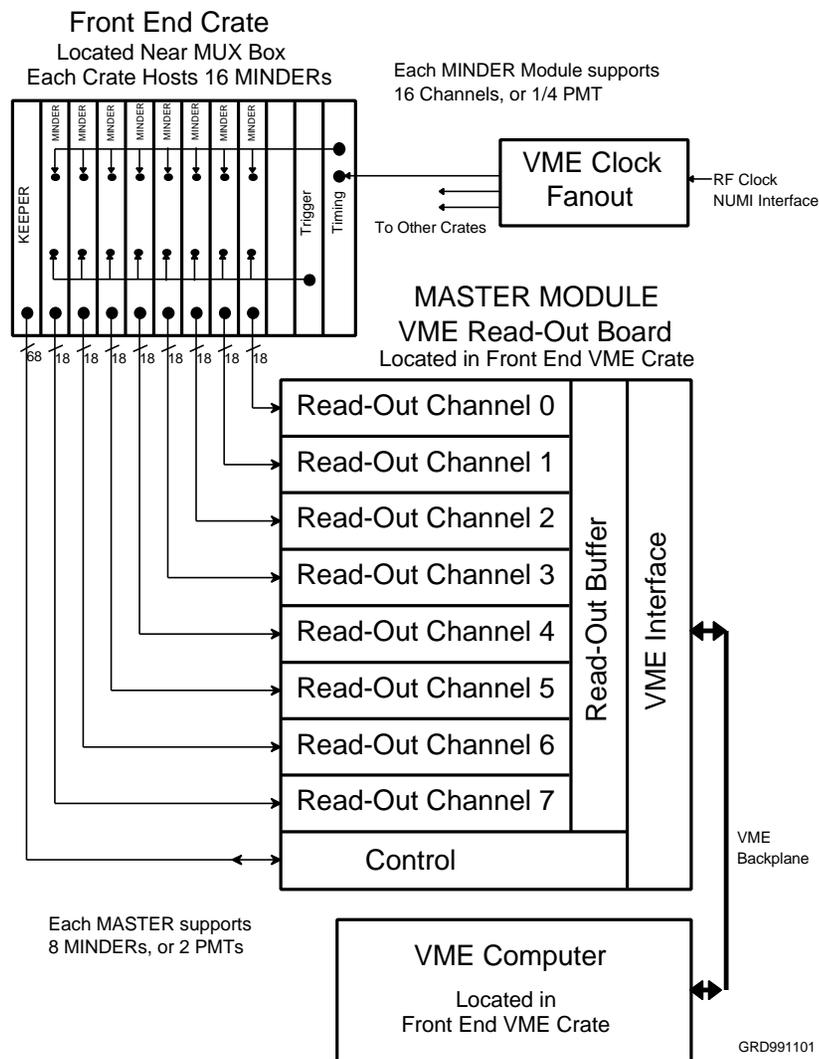
➤ VME Readout Crate

- Data Collection and Concentration
- Zero Suppression
- Interface to DAQ System



System Description

System Block Diagram





System Description

Description of System Components

- **The QIE**

- Custom IC Based on KTeV & CDF QIEs
- “Current Splitter” with Gated Integrator
- 53 MHz Operation
- “Deadtimeless” Digitization
- Pipelined Operation



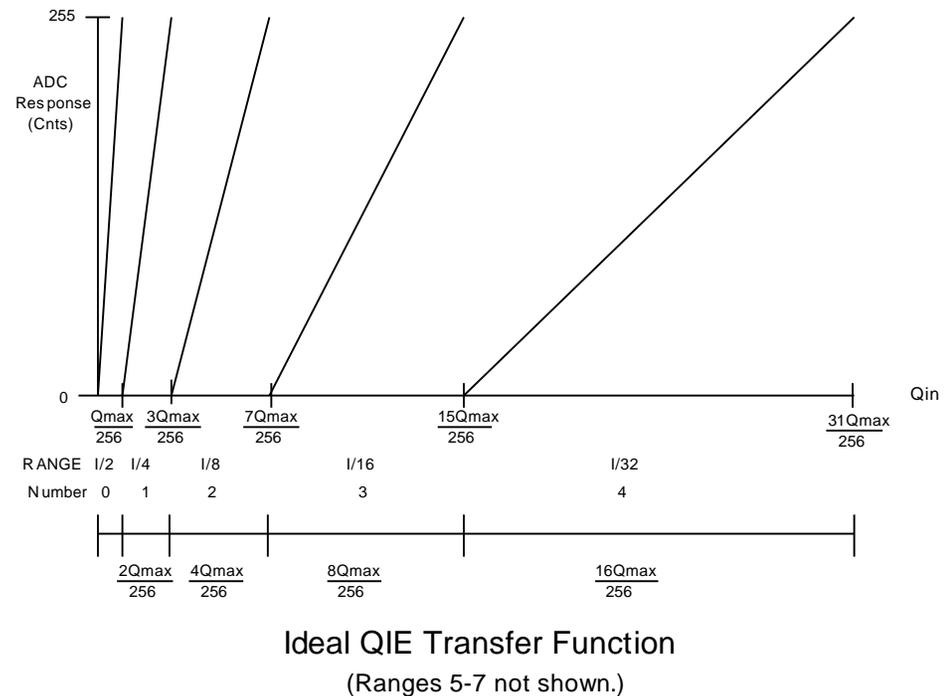


System Description

Description of System Components (Cont.)

• The QIE (Cont.)

- Splits Current into Binary Ranges & Integrates Charge
- Signal on 1 Range is Output for Digitization by External ADC
- Creates Floating Point Format



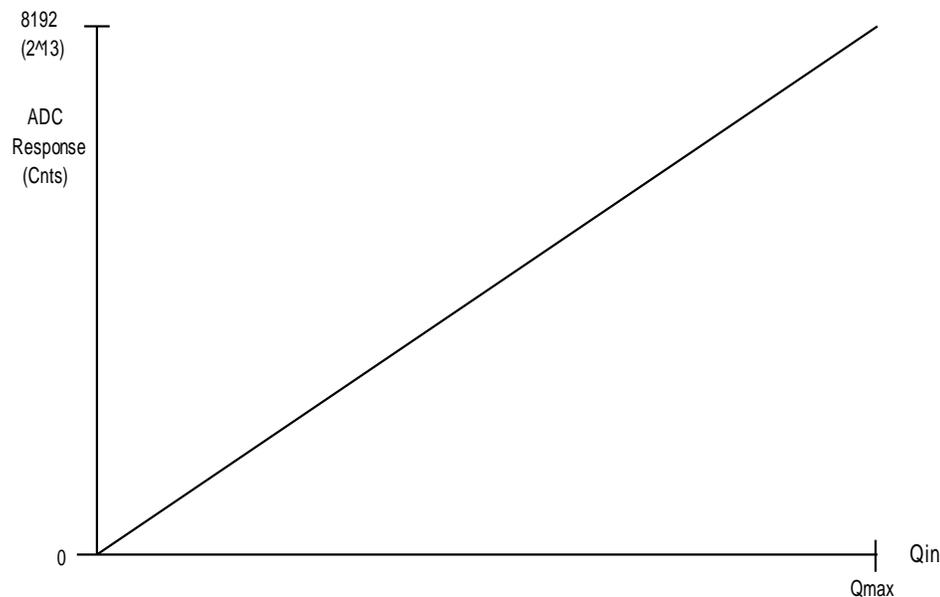


System Description

Description of System Components (Cont.)

- **The QIE (Cont.)**

- Data Must be “Linearized”
 - Operation Done in MASTER Using Look-Up Tables (LUTs)

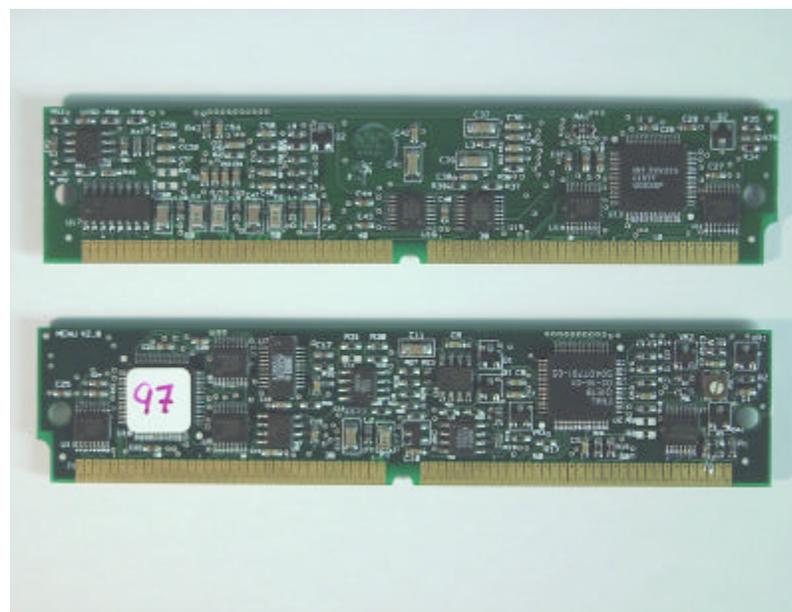




System Description

Description of System Components (Cont.)

- **The MENU Module**
 - Based on CDF Designs (CAFÉ & SQUID)
 - Mount QIEs on SIMM Boards
 - Performs All Analog Processing & Digitization



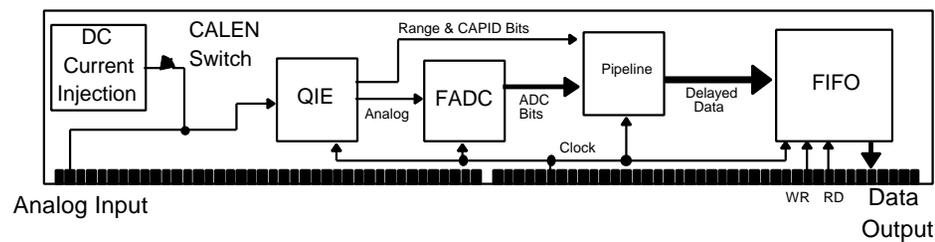


System Description

Description of System Components (Cont.)

• The MENU Module (Cont.)

- Has 8-Bit FADC
- Has On-Board DC Current Injection Circuit for Calibrations
- Contains Digital Pipeline to Give Time to Form Triggers
- Contains Temporary Storage of Data





System Description

Description of System Components (Cont.)

- **The MINDER Module**

- Similar to CDF Shower Max Design (SMD)
- 6U Format
- Holds 16 MENU Modules
- (1/4) 16-Channel PMT
- Reside in Crates Close to Photodetectors



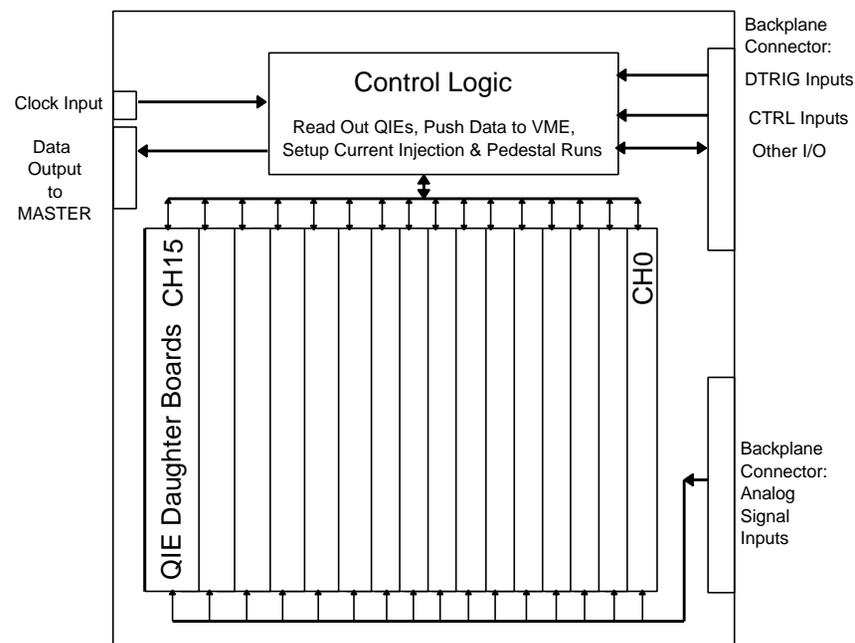


System Description

Description of System Components (Cont.)

• The MINDER Module (Cont.)

- Processes Triggers
- Pushes Data to MASTER
- Contains 27-Bit Timestamp Counters
- Sets Up DC Current Calibration
- Contains Pre-Programmed Diagnostic Data



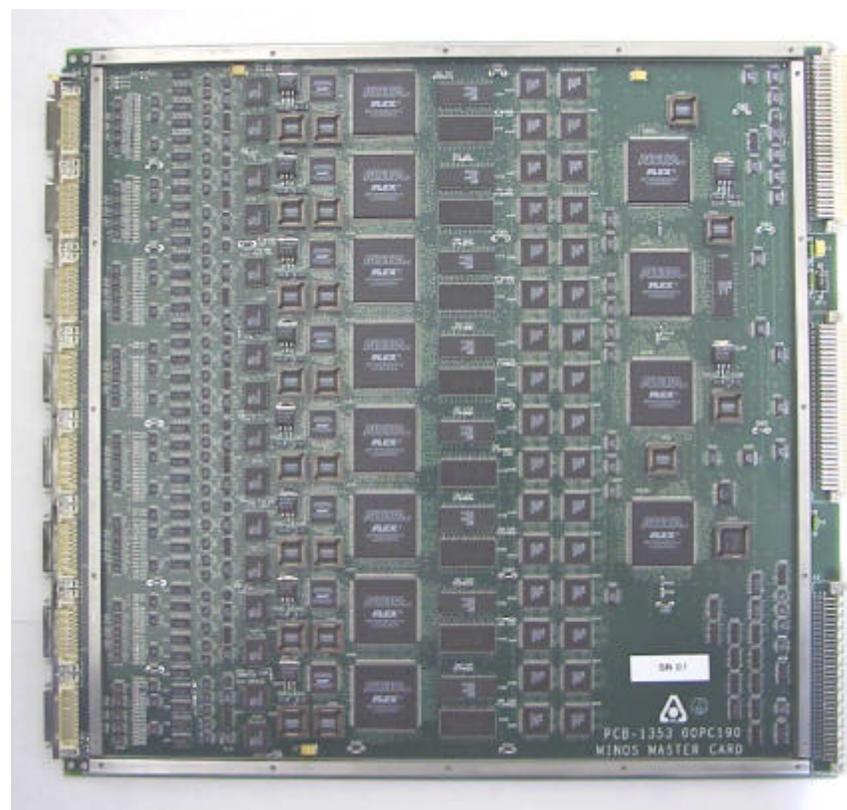


System Description

Description of System Components (Cont.)

• **The MASTER Module**

- Similar to CDF Shower Max Design (SMXR)
- 9U x 400 mm Format
- Interfaces to 8 MINDER Modules
- Receives and Processes Data from MINDERS
- Controls Operations in Front End Crate





System Description

Description of System Components (Cont.)

• **The MASTER Module (Cont.)**

- “Linearizes” QIE Data through LUTs
- Performs Zero Suppression
- Append Timestamp & Channel ID to Data
- Save Data in Readout Buffers
- Two Readout Buffers, Alternate Read & Write
- Controls Operations in MINDER Crate through Simple Communication Link with KEEPER

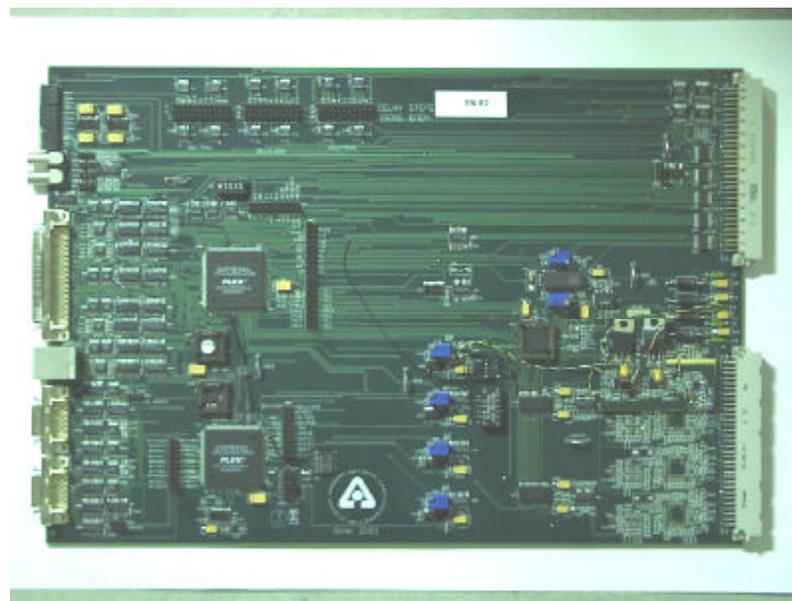


System Description

Description of System Components (Cont.)

- **The KEEPER**

- MINDER Crate is a VME Crate, but No VME Protocol
- KEEPER is Crate Controller for MINDER Crate
- Slave to MASTER - No Intelligence





System Description

Description of System Components (Cont.)

- **The KEEPER (Cont.)**

- Contains DAC for Calibrations (1 DAC per MINDER Crate)
- Contains Interface to MINDER Backplane
- Contains Discriminators for PMT Dynodes, Used for Cosmic Ray Mode and Resonant Extraction Mode
- Sophisticated Triggering Possible



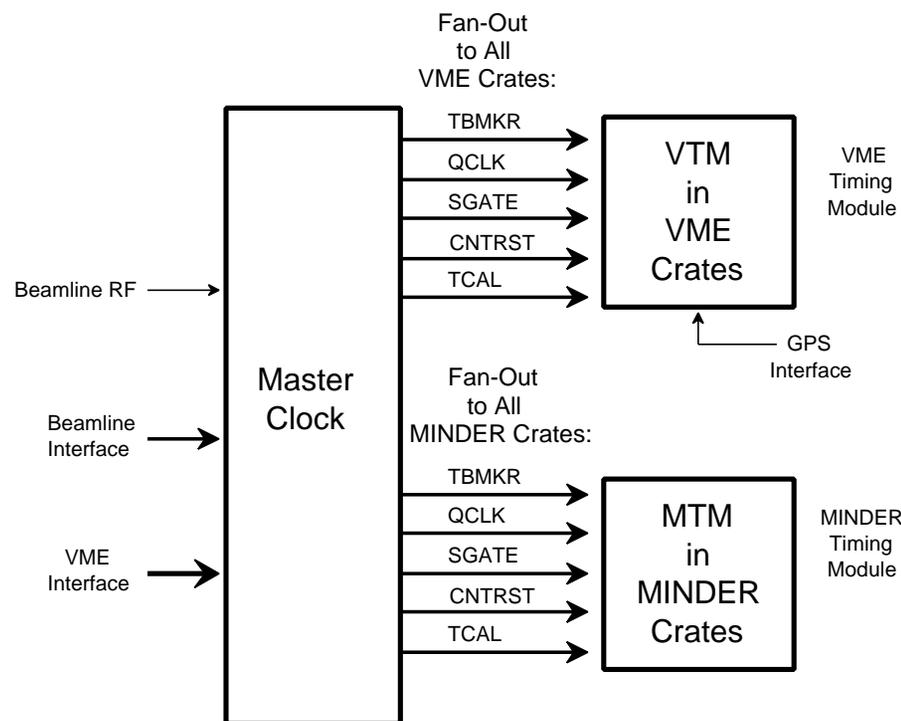
System Description

Description of System Components (Cont.)

• The Clock System

➤ 3 Primary Parts:

- Master Clock - Source & Control of All Timing Signals
- VTM - Controls Timing in VME Readout Crate
- MTM - Controls Timing in MINDER Crate





System Description

Description of System Components (Cont.)

• The Clock System (Cont.)

➤ Primary Clock Signals:

- QCLK – 53 MHz Clock for QIEs
 - Create RF/2 for Data Transmission
- SGATE – Spill Gate, Indicating SPILL In Progress
- CNTRST – Reset Timestamp Counters, Everywhere Simultaneously
- TBMKR – Time Block Marker
 - Controls Readout Buffer Swap in MASTER
 - Used by ROP to Create Time Frames
- TCAL – Used to Charge Inject into Discriminators
 - Used by Flasher System to Flash LEDs



System Description

Description of System Components (Cont.)

• The Clock System (Cont.)

➤ Master Clock

- Receive & Fan Out RF Clock to VME & MINDER Crates
- Receive & Fan Out Spill Gate
- Generate Programmable Timing Signals Needed by System, Synchronized to RF Clock

➤ VTM

- Provides SYSCLK for VME Crate
- Real-time Timestamp of Spill Gate Using GPS

➤ MTM

- Provides QIE Clock & Spill Gate for MINDER Crate



Hardware Responsibilities

- MENU - FNAL (Charlie Nelson)
- MINDER - ANL (Gary Drake, Tim Cundiff)
- MASTER - ANL (John Dawson, Bill Haberichter)
- KEEPER - ANL (John Dawson, Bill Haberichter)
- Master Clock - FNAL (Tom Fitzpatrick)
- MTM - FNAL (Tom Fitzpatrick)
- VTM - IIT (Bill Luebke, Chris White)



References

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- [6] G. Drake, T. Fitzpatrick, C. Nelson, C. Rotolo, "Technical Requirements for the MINOS Near Detector Master Clock," NUMI Internal Note NUMI-NOTE-ELEC-826, Feb. 11, 2002.
- [7] T. Fitzpatrick, C. Rotolo, "MINOS Master Clock System Preliminary Design Specification," NUMI Internal Note NUMI-NOTE-ELEC-827, December 6, 2000.
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