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# MINOS Near Detector Front End Electronics Tutorial

## Description of the MENU Module

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# Description of the QIE

## Overview

### • **Some Background**

- Custom IC Based on KTeV & CDF QIEs
- QIE7 - “7th Generation”
- Designed at FNAL
- Mixed NPN Bipolar and CMOS Transistors
- 2.0 micron Feature Size, Low-Noise Analog Process





## Description of the QIE

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### Overview (Cont.)

- **What it Does**

- Receives Charge from PMT Anode
- “Splits” Charge into Binary-Weighted Ranges
- Integrates Charge Fractions on Separate Capacitors
- Selects (Somehow) One Range to be Digitized
- Outputs the Analog Voltage from the Selected Range, and a Digital Representation of the Range Number (0 - 7, 3 Bits)



# Description of the QIE

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## Overview (Cont.)

### • What it Does (Cont.)

- Operates at 53 MHz (19 nS period)
- Operation is *Deadtimeless*
  - Every Clock Cycle, a New Sample is Presented at the Output
  - Always Live for Sampling Input
- Operations are *Pipelined* to Achieve No Deadtime
- Digitization is Done Externally, Not Part of Chip



# Description of the QIE

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## Principles of Operation

### • 4 Phases of Operation

- Integrate
- Compare & Range Select
- Output Analog Voltage (Digitize)
- Reset



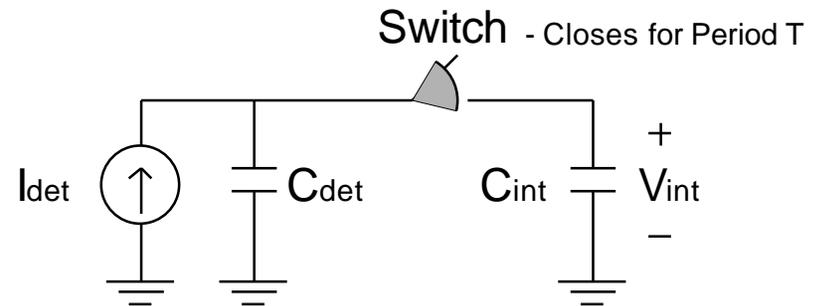
## Description of the QIE

### Principles of Operation (Cont.)

#### • Integrate Phase

##### ➤ Basic Gated Integrator:

- Close Switch for Period T
- Collect Charge on a Capacitor
- Collected Charge Creates a Voltage
- ADCs Digitize Voltage



$$I_{det}(t) = C_{int} \frac{dV_{int}(t)}{dt}$$

$$V_{int} = \frac{1}{C_{int}} \int_0^T I_{det}(t) dt$$



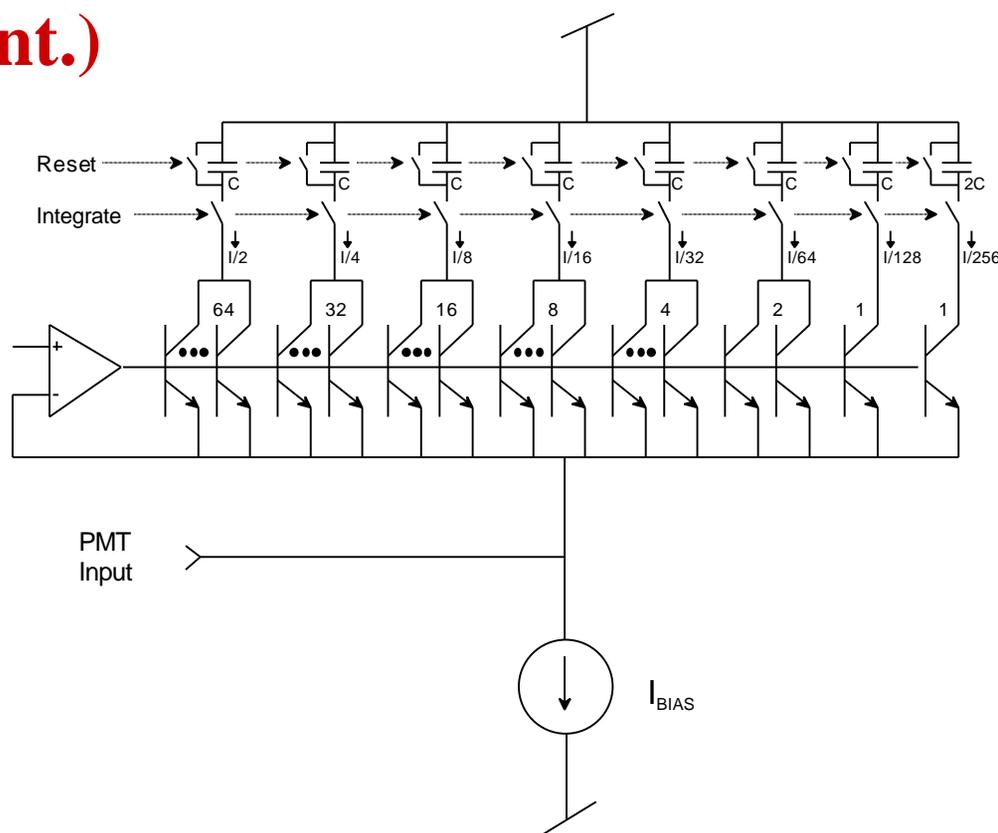
# Description of the QIE

## Principles of Operation (Cont.)

### • Integrate Phase (Cont.)

➤ QIE Uses Current Splitter:

- 128 Identical Transistors
- Emitters All Common to Input
- Collectors Grouped in Binary Numbers
- Collectors Connected to Gated Integrators  
→ *Ranges*





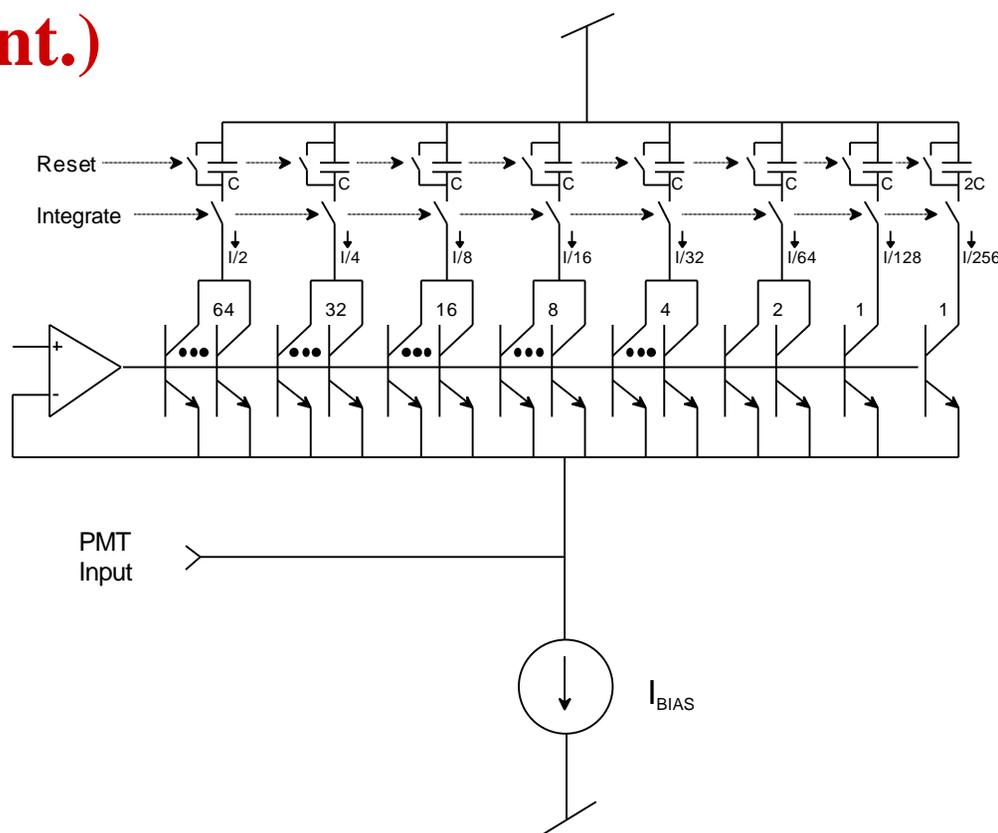
# Description of the QIE

## Principles of Operation (Cont.)

### • Integrate Phase (Cont.)

➤ QIE Uses Current Splitter (Cont.):

- $1/2$  of  $I_{BIAS}$  Goes Onto  $I/2$ ,  
 $1/4$  of  $I_{BIAS}$  Goes on  $I/4$ , etc.
- Voltage Proportional to Integrated Current:  
 $V_2 = 2V_4 = 4V_8$  etc.





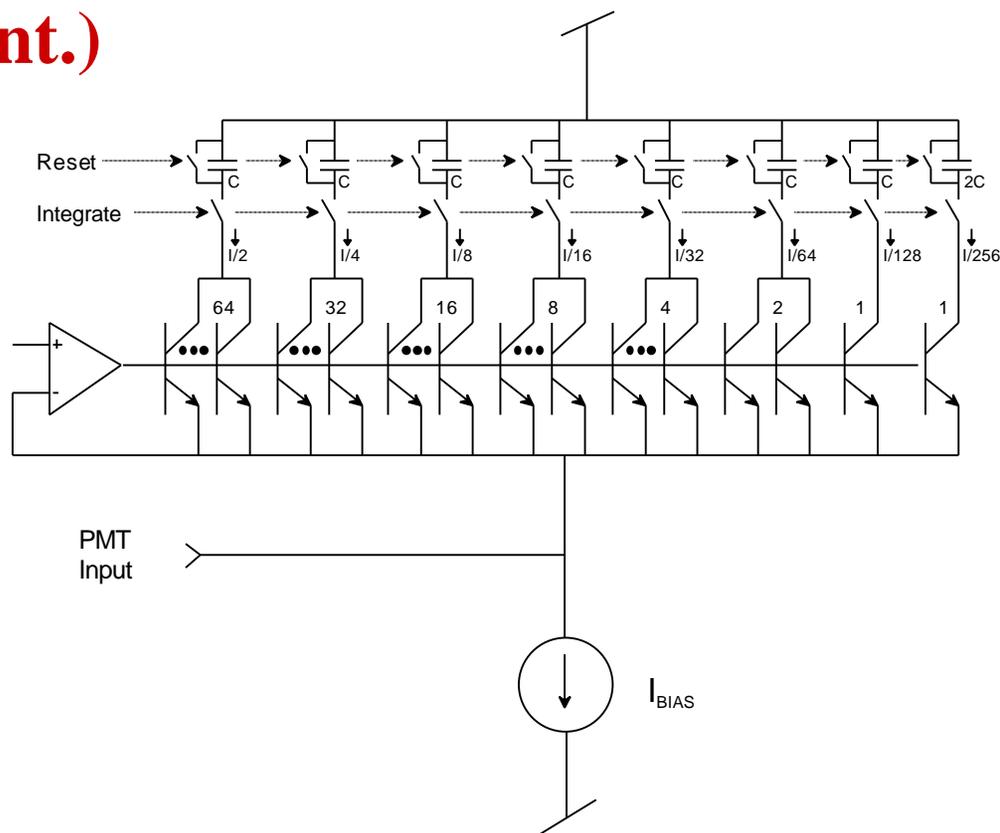
# Description of the QIE

## Principles of Operation (Cont.)

### • Integrate Phase (Cont.)

➤ QIE Uses Current Splitter (Cont.):

- Last 2 Stages Each Draw  $I/128$  of Current
- $V_{128} = 2V_{256}$  Because  $C_{256} = 2C_{128}$





# Description of the QIE

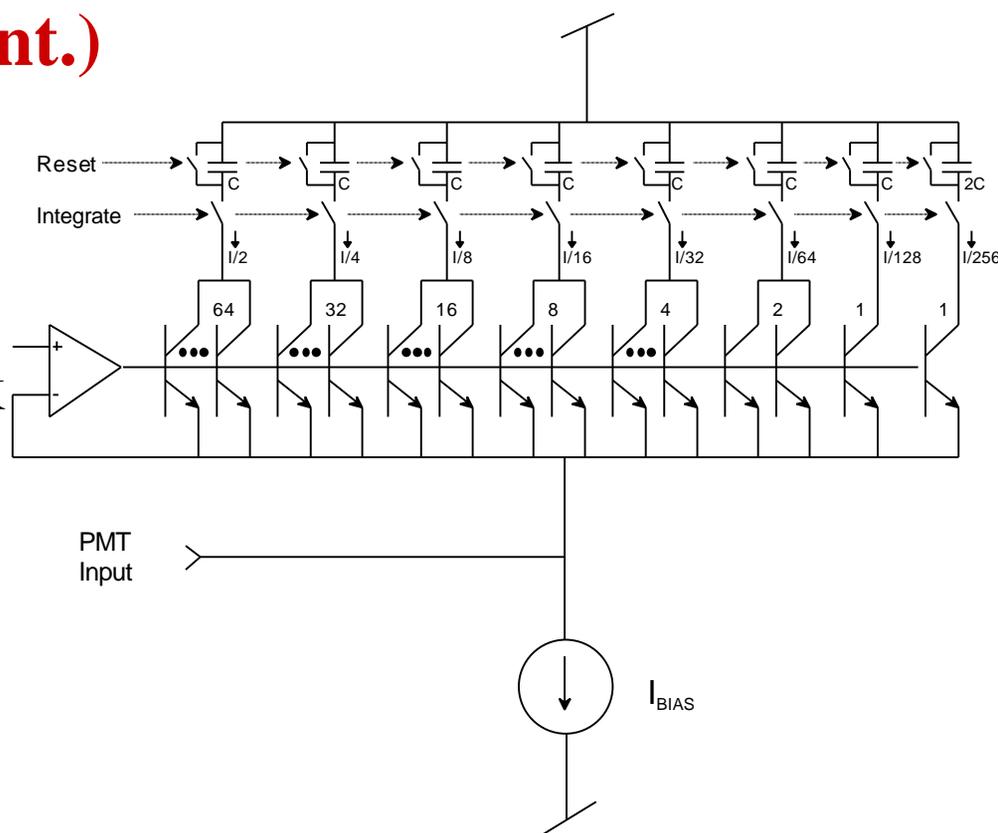
## Principles of Operation (Cont.)

### • Integrate Phase (Cont.)

➤ Voltages From  $I_{BIAS}$  Splitting Creates “Pedestals”

➤ At End of 19 nS Clock Cycle (at Pedestal):

- $V_2 = 1\text{ V}$
- $V_4 = 0.5\text{ V}$
- $V_8 = 0.25\text{ V}$  etc.



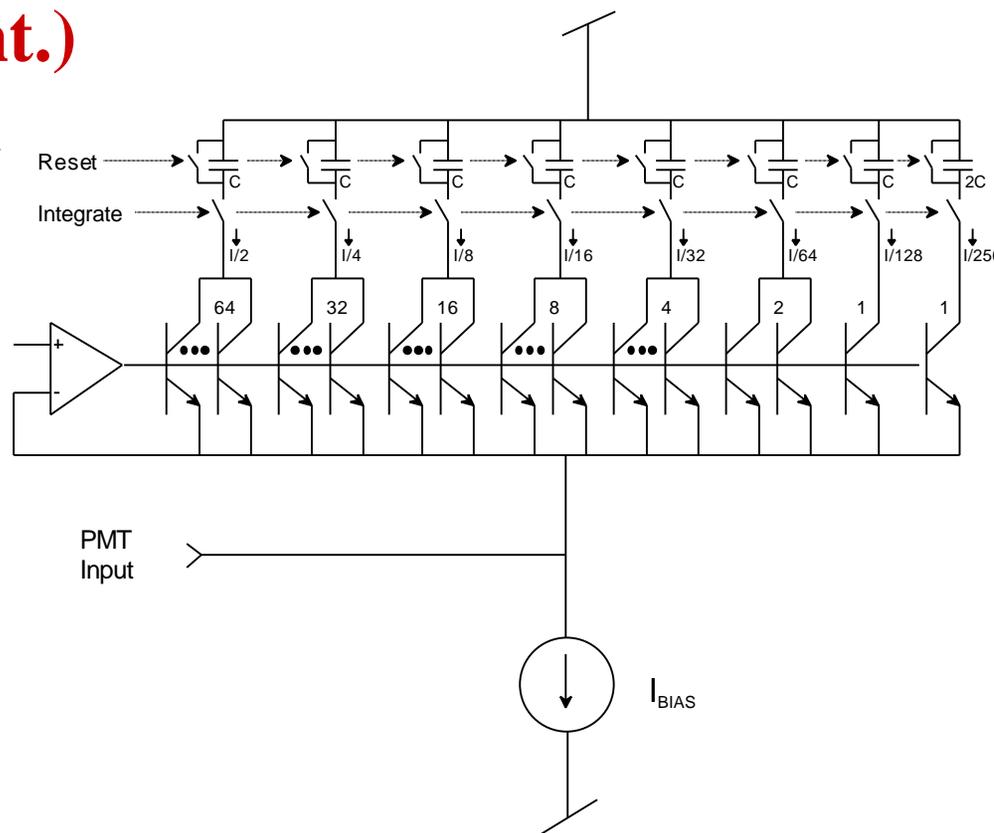


# Description of the QIE

## Principles of Operation (Cont.)

### • Integrate Phase (Cont.)

- Additional Current from PMT Splits the Same Way, and Adds Voltage to Each Capacitor
- At End of 19 nS Clock Cycle (Ped + PMT Sig):
  - $V_2 = 1 \text{ V} + Q_{\text{PMT}} / 2C$
  - $V_4 = 0.5 \text{ V} + Q_{\text{PMT}} / 4C$
  - $V_8 = 0.25 \text{ V} + Q_{\text{PMT}} / 8C$
  - etc.



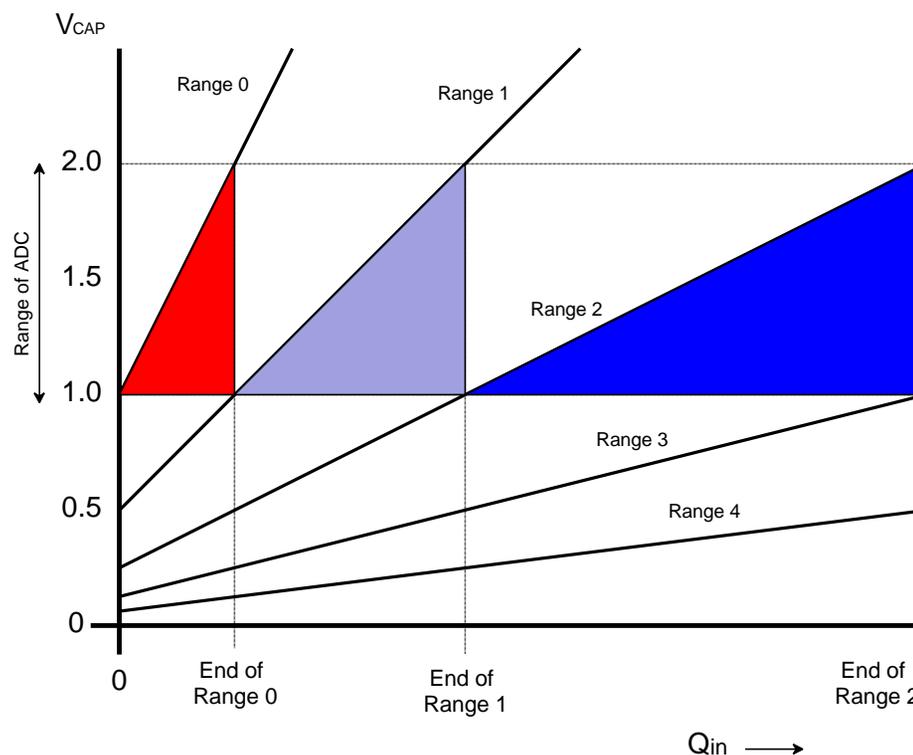


# Description of the QIE

## Principles of Operation (Cont.)

### • Compare Phase

- Principle: **One and only One** Capacitor Voltage is Within Range of (External) ADC
- Range of ADC is 1V to 2V:
  - 1V = 0 ADC Counts
  - 2V = 255 Counts



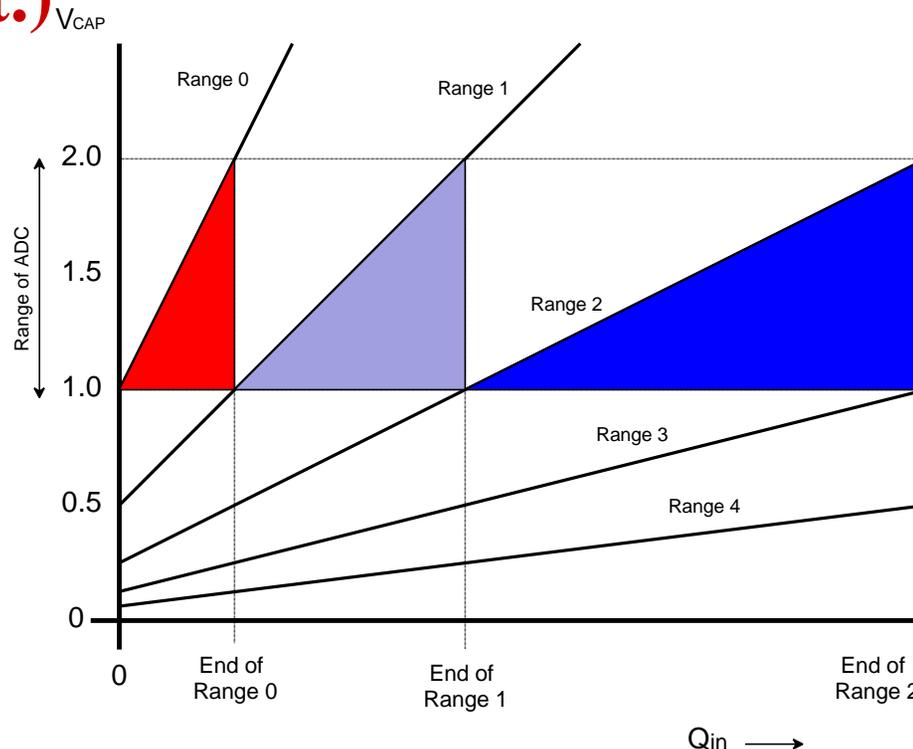


# Description of the QIE

## Principles of Operation (Cont.)

### • Compare Phase (Cont.)

- Range Comparison  
Circuitry Inside QIE  
Selects Appropriate  
Capacitor for Output
- Circuitry Also Outputs  
Binary Representation  
of Selected Range



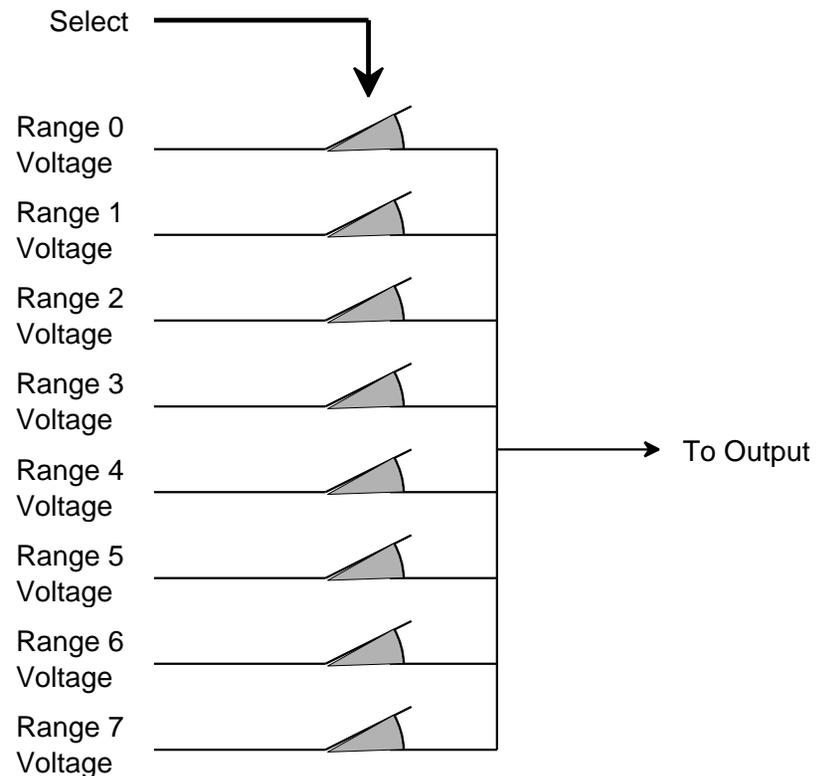


# Description of the QIE

## Principles of Operation (Cont.)

### • Output Phase

- Range Comparison  
Circuitry Inside QIE  
Selects Appropriate  
Capacitor for Output
- Circuitry Also Outputs  
Binary Representation  
of Selected Range
- Output Goes to External  
FADC, Which Digitizes  
at End of Output Cycle



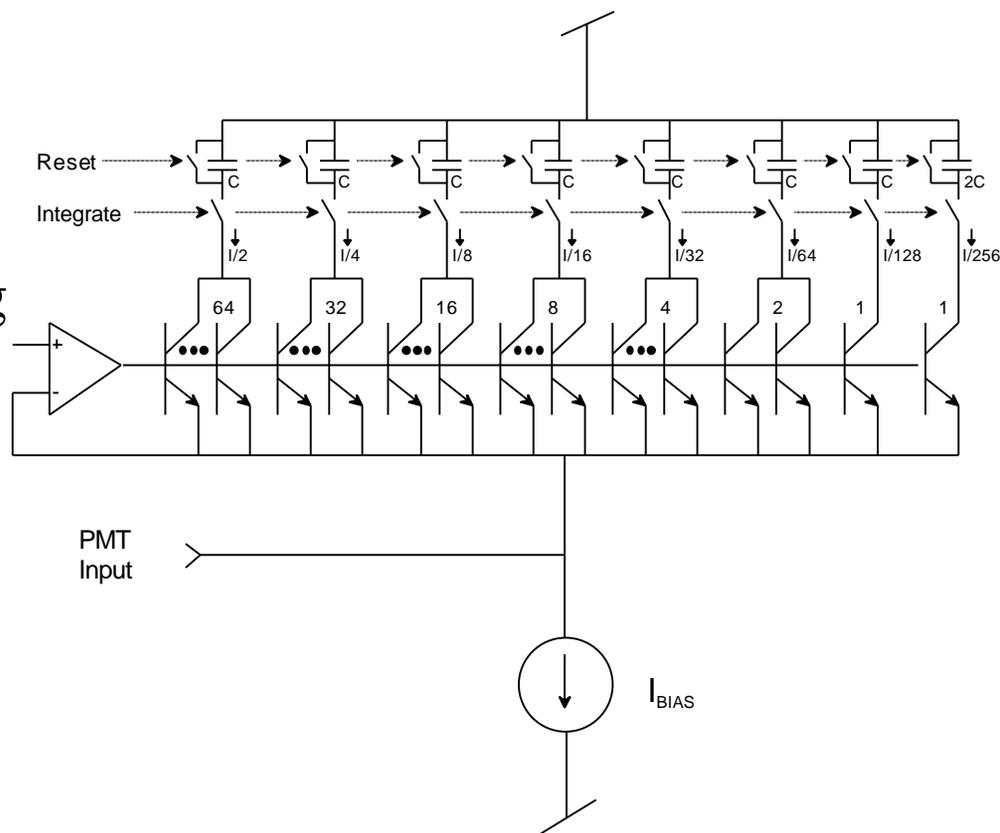


# Description of the QIE

## Principles of Operation (Cont.)

### • Reset Phase

- After Digitization, Integrating Capacitors are Cleared by Closing Reset Switch





## Description of the QIE

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### Principles of Operation (Cont.)

- **Why No Deadtime?**

- 4 Clock Cycles Needed to Produce an Output:

- 1 Clock for **Integrate**
- 1 Clock for **Compare**
- 1 Clock for **Output**
- 1 Clock for **Reset**

- *Why is QIE Not Dead 75% of Time???*

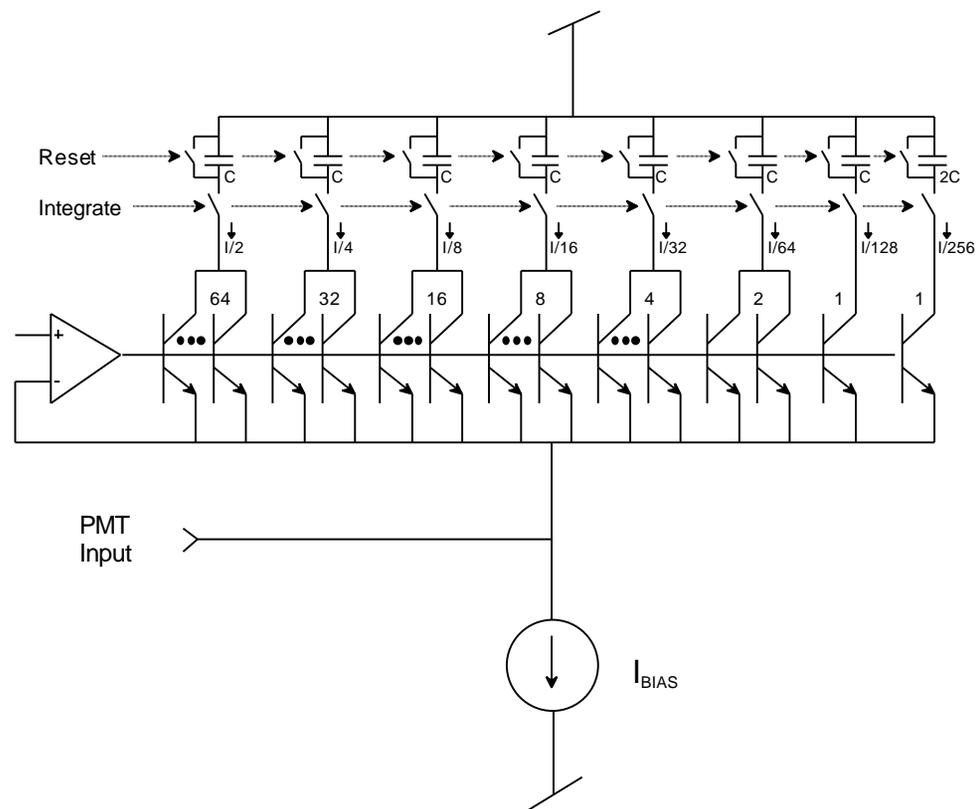
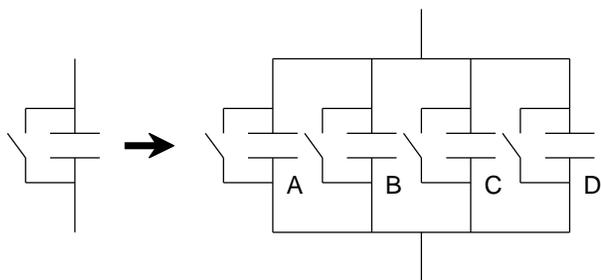


# Description of the QIE

## Principles of Operation (Cont.)

### • Why No Deadtime?

➤ *Answer:* Every Capacitor Actually has **4 Capacitors**



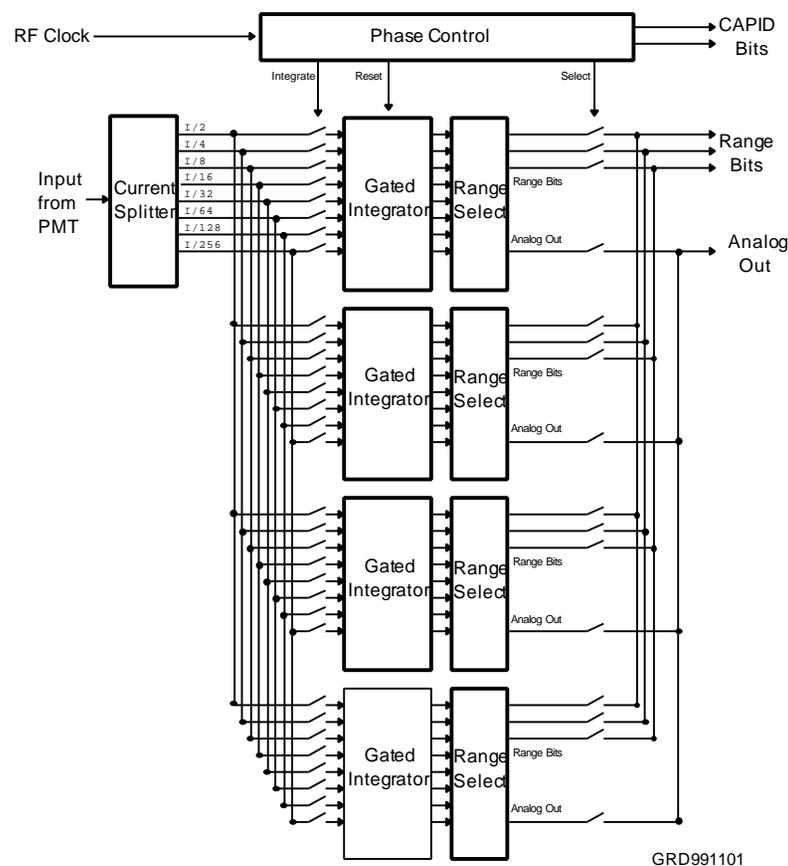


# Description of the QIE

## Principles of Operation (Cont.)

### • 4-Phase Clock

- Think of Having 4 Sets of Gated Integrators
- At Any Given Time:
  - One Set in Integrate Phase
  - One Set in Compare Phase
  - One Set in Output Phase
  - One Set in Reset Phase
- Roles Change on Each Clock Cycle



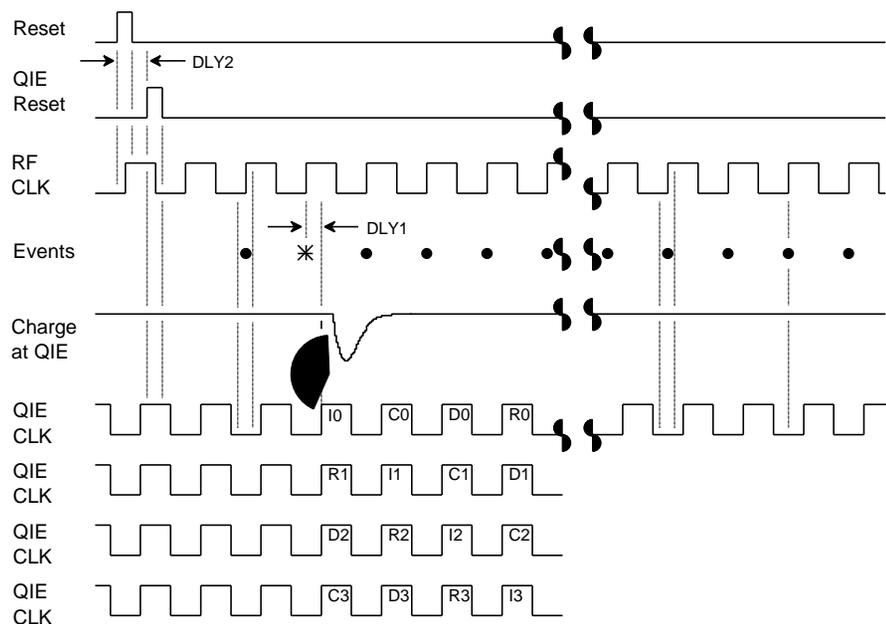


# Description of the QIE

## Principles of Operation (Cont.)

### • 4-Phase Clock (Cont.)

- Think of 4 Clocks, Each Out of Phase From an Adjacent One by One Clock Cycle
- The 4-Phase Clock is Generated Inside the QIE



I=Integrate  
 C=Compare  
 D=Digitize  
 R=Reset



## Description of the QIE

### Principles of Operation (Cont.)

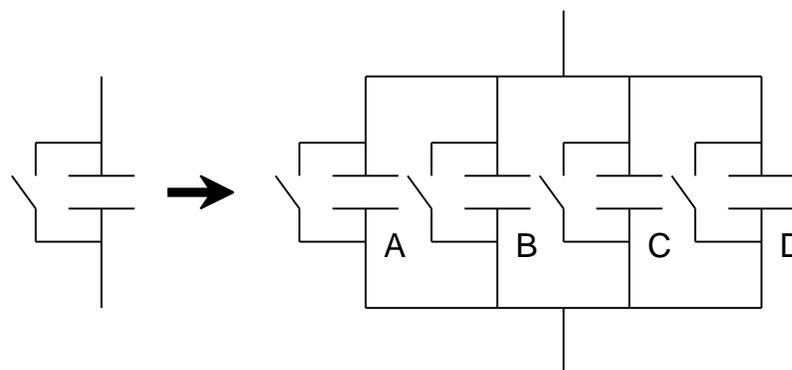
#### • 4-Phase Clock (Cont.)

➤ Scheme Relies on Good Matching of Capacitors

- In CMOS, Capacitors Match to ~ Few %
- Can Calibrate Out Differences

→ *Capacitor IDs*

➤ QIE Outputs 2 CAPID Bits During Output Phase, to Indicate Bank





## Description of the QIE

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### Principles of Operation (Cont.)

- **Summary**

- QIE Splits Input Current, Integrates Fractions Separately
- Outputs Analog Voltage, Corresponding Range Bits (3), and CAPID Bits (2)
- It *Never* Stops! (As Long As There is a Clock.)
- External 8-Bit FADC Digitizes Output Voltage

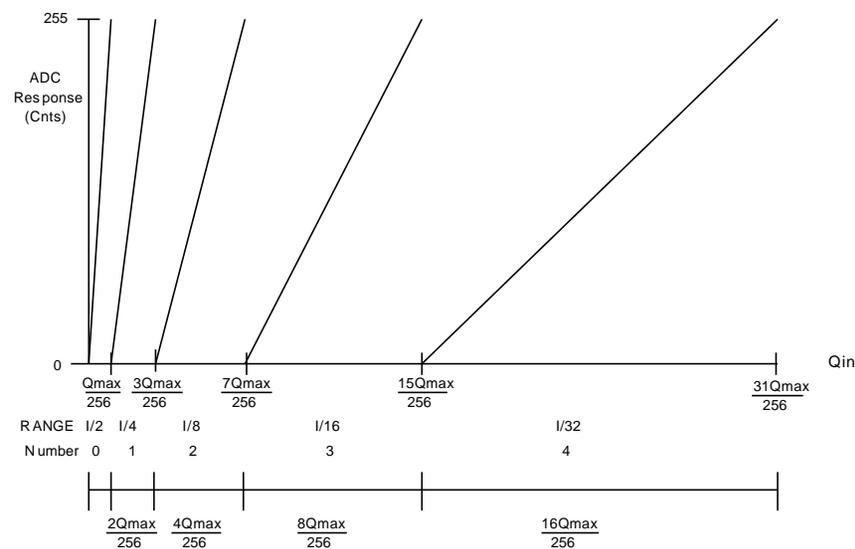
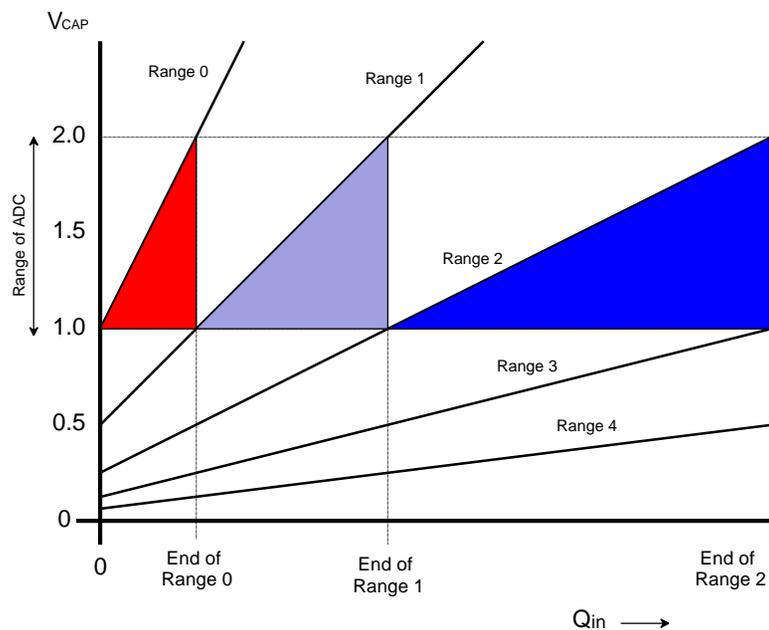


# The MENU Module

## Principles of Operation

### • The QIE Transfer Function

➤ Recall Range Comparison



Ideal QIE Transfer Function  
 (Ranges 5-7 not shown.)



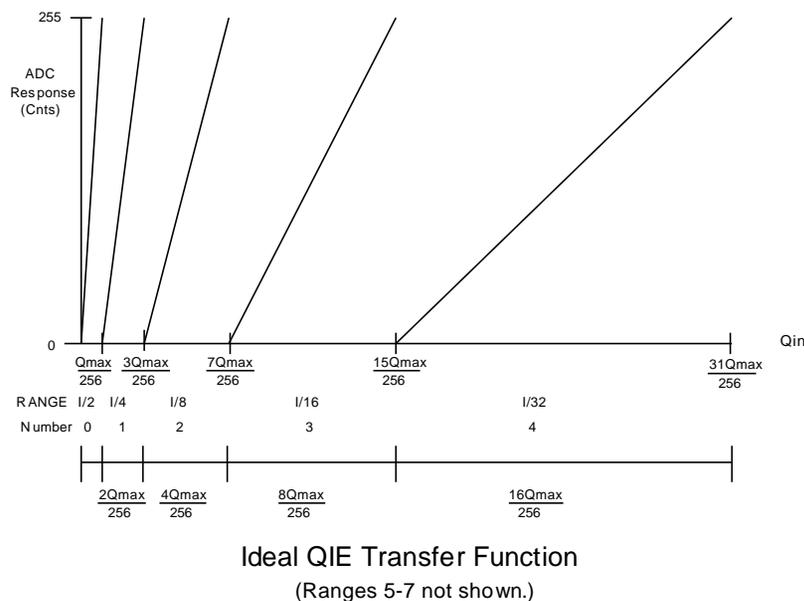
MINOS

# The MENU Module

## Principles of Operation

### • The QIE Transfer Function (Cont.)

- Digitization Begins on Range 0, Near  $ADC = 20$  (Offset Added by Analog Circuitry)
- As Increase Charge, ADC Value Increases
- At Top of Range 0,  $ADC = \sim 250$



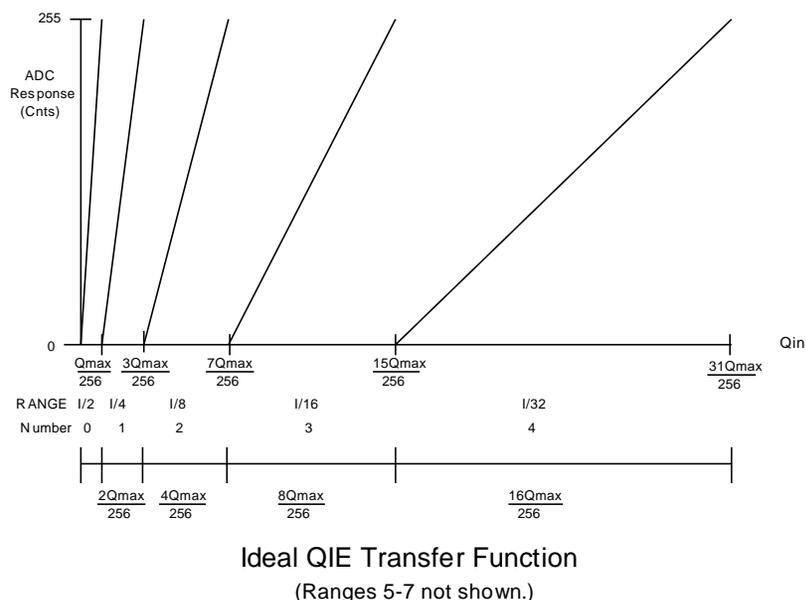


# The MENU Module

## Principles of Operation

### • The QIE Transfer Function (Cont.)

- When at Top of Range 0, QIE Switches to Range 1  
→ Analog Output Falls, & ADC Output ~ 20 Again
- Gives “Sawtooth” Response  
→ Piecewise-Linear  
→ Key to Calibrations



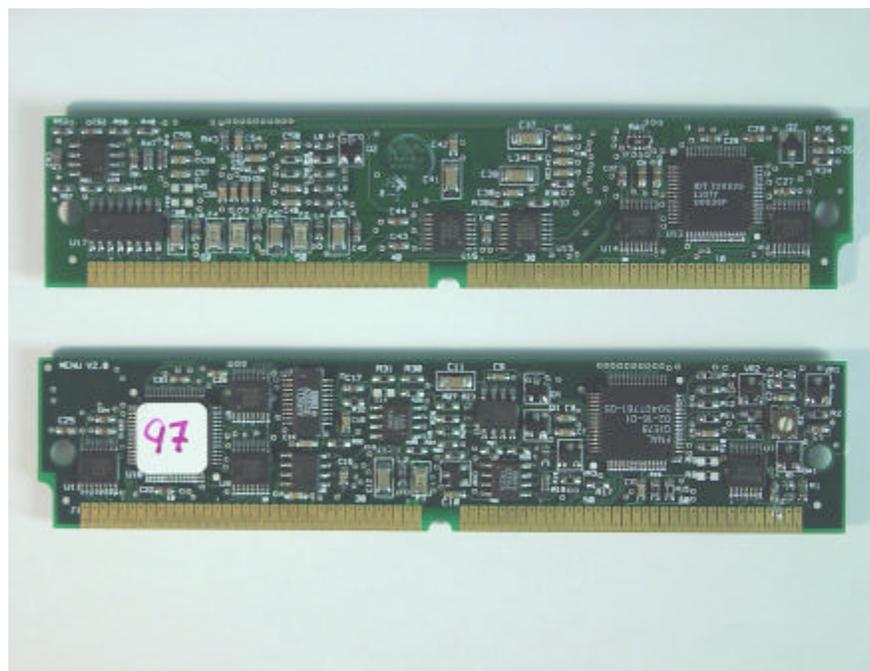


# The MENU Module

## Overview

### • Some Background

- Based on CDF Designs (CAFÉ & SQUID)
- Memory SIMM Format
- In Addition to QIE, It Contains
  - 8-Bit FADC & Support
  - Data Pipeline
  - Output FIFO
  - Calibration Circuitry



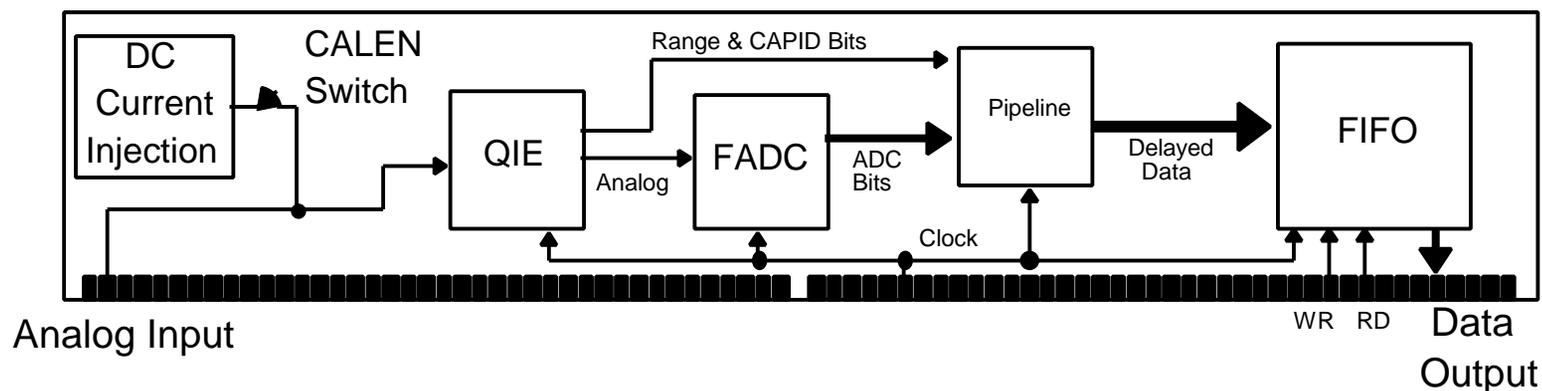


# The MENU Module

## Overview (Cont.)

### • What it Does

- Performs All Analog Processing & Digitization
- Contains Data Pipeline for Aligning ADC & QIE Bits (There is a Lag...)



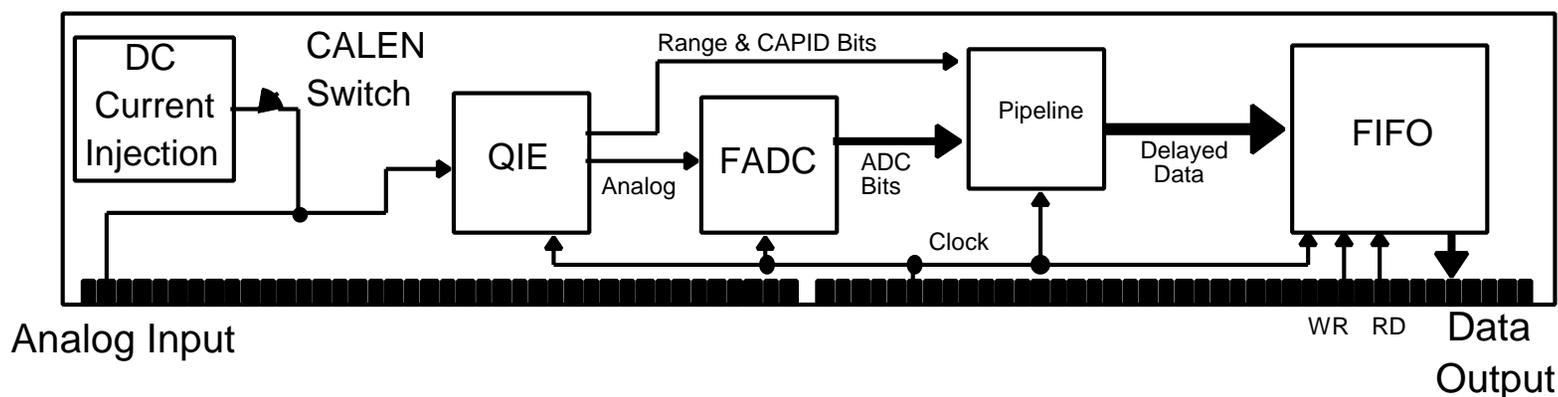


# The MENU Module

## Overview (Cont.)

### • What it Does (Cont.)

- Contains 1K FIFO for Storage of Data Accepted by a Trigger
- Contains Circuitry for Performing DC Current Injection for Calibrations



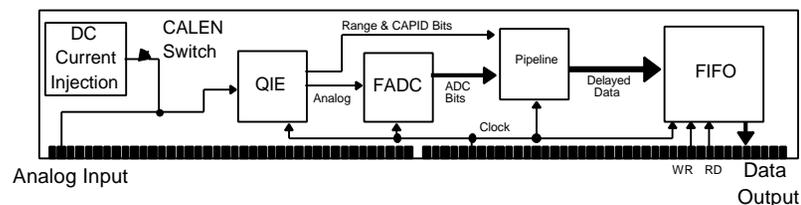


# The MENU Module

## Principles of Operation

### • The FADC

- FADC Digitizes to 8 Bits – 0.4% Precision
  - The FADC Receives Analog Voltage from QIE During Output Phase (There is an Output Phase on Every Clock Cycle...)
  - Digitization Sequence Begins at *End* of Clock Cycle
  - Digitization Sequence Requires 4 Clock Cycles
- Pipelined Operation Inside FADC



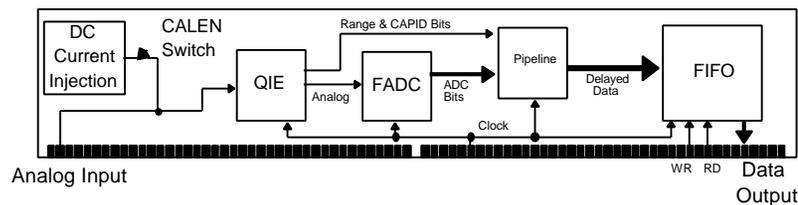


# The MENU Module

## Principles of Operation (Cont.)

### • The Pipeline

- QIE Bits (3 Range Bits & 2 CAPID Bits) Output at the Beginning of the Output Phase (There is an Output Phase on Every Clock Cycle...)
- Digitization Sequence Requires 4 Clock Cycles  
→ Need Alignment Pipeline to Delay QIE Bits





# The MENU Module

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## Principles of Operation (Cont.)

- **The Pipeline (Cont.)**

- Pipeline Also has 4 Extra Stages of Delay, to Provide Extra Time for Trigger Formation
  - Total Latency:
    - 2 QIE Cycles (Integrate & Compare)
    - 4 FADC Clock Cycles
    - 4 Extra Pipeline Stages
- QIE Word Available *10 Clocks* After Charge Received

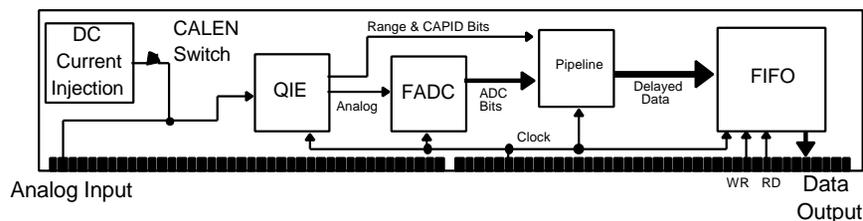


# The MENU Module

## Principles of Operation (Cont.)

### • The FIFO

- Data Stored in 1K FIFO
- Write Enable Timed to Capture Data of Interest
  - ~8 Clock Cycles Latency for Dynode Trigger
  - 8 Clock Window for Dynode Trigger
  - 526 Clock Window for STE Spills
- FIFO is Read *After* Write Cycle is Completed





# The MENU Module

## Principles of Operation (Cont.)

### • DC Current Injection

- Uses Voltage-to-Current Converter, Switched In & Out
- External Precision DAC Supplies Voltage (From KEEPER)
- Conversion: 1 Volt  $\alpha$  1 mA  $\alpha$  ~19 pC

