

MINOS

NuMI-NOTE-ELEC-826

**Technical Requirements
for the
MINOS Near Detector
Master Clock**

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Version 2.1

Feb. 11, 2002

Contents

1. Introduction	p. 3
2. Description of Primary Timing Signals	p. 6
2.1 QIE Clock (QCLK)	p. 6
2.2 Spill Gate (SGATE)	p. 7
2.3 Counter Reset (CNTRST)	p. 8
2.4 Time Block Marker (TBMKR)	p. 9
2.5 Timing Calibration (TCAL)	p. 10
2.6 Hold-Off Conditions	p. 11
3. Technical Specifications	p. 12
3.1 General Parameters	p. 12
3.2 Inputs to Master Clock	p. 14
3.3 Generation of QCLK	p. 15
3.4 Generation of SGATE	p. 17
3.5 Generation of CNTRST	p. 18
3.6 Generation of TCAL	p. 19
3.7 Generation of TBMKR	p. 20
4. Bibliography	p. 21

1. Introduction

The front end electronics for the MINOS Near Detector has two parts. The Front End Crate is a 6U crate that is located close to the MUX Boxes. This crate contains the QIE Digitizers, which operate with a 53 MHz clock. The QIEs digitize charge signals from phototubes, which form the primary detector system of the MINOS experiment. When data is digitized by the QIEs, it is held in local memories on the QIE motherboards boards called MINDER Modules, that reside in the Front End Crate. Each MINDER Module forms a timestamp on the data that it acquires to aid in reconstruction of events across the detector. After data is acquired, it is transferred from these memories to boards called MASTER Modules, which reside in 9U VME Readout Crates. In each Readout Crate, there also resides a VME Processor. After data is sent to the MASTER Module, it is processed and stored locally, pending readout by the processor.

The DAQ system will be able to operate in three different modes:

- (1) *Single Turn Extraction Mode.* The trigger is a spill signal from the Main Injector. Data will be collected for every RF bucket during the 10 microsecond spill and will be stored in FIFOs on front-end cards. Collection of data from the front-end FIFOs will be deferred until after the spill. The Data Acquisition (DAQ) system will receive zero-suppressed data. Events will be time-stamped according to the RF bucket with which they are associated This mode is dead-timeless, with respect to the spill time.
- (2) *Cosmic Ray Mode.* Cosmic ray data will be collected during the one or two second intervals between spills. Data from a few RF buckets will be stored on receipt of a local, prompt trigger (e.g., a discriminated dynode signal). Front-end FIFOs will be read out as soon as data is available. The DAQ system will receive zero-suppressed data. Dead-time will be small.
- (3) *Resonant Extraction Mode.* As in Cosmic Ray Mode, data from a few RF buckets will be stored on receipt of a trigger from a dynode discriminator, but FIFO readout will be deferred until the end of the spill. The DAQ system will receive zero-suppressed data. This mode will be dead-timeless as long as FIFOs do not overflow.

For the purposes of this document, the active period in which protons are delivered from the Main Injector to the target is called the "spill," whether the operation is Single-Turn Extraction or Resonant Extraction. A description of the system components and the principles of operation are given in [1].

The front end electronics has a Clock System, which provides timing and control for both the VME Readout Crates and the Front End Crates. The Clock System has three primary components: the Master Clock; the VME Timing Module (VTM); and the MINDER Timing Module (MTM). A block diagram of the system is shown in Fig. 1.

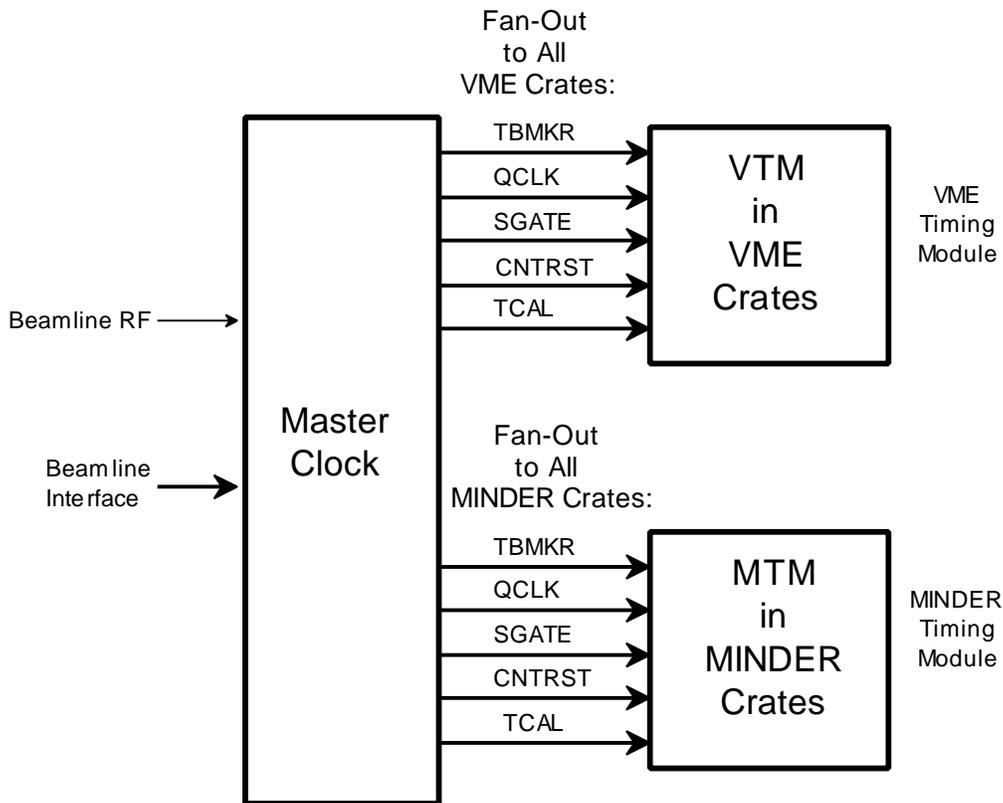


Fig. 1. Block Diagram of Clock System

The system components are:

- **The Master Clock**

The Master Clock is the source of all global timing signals in the system. It receives signals from the Main Injector Control System, and processes them to form timing signals needed to operate the electronics. The timing signals are fanned out to the VME Readout Crates and the Front End Crates. There is one Master Clock in the system, although it may have several sub-components.

- **The VME Timing Module (VTM)**

A VME Timing Module resides in each VME Readout Crate. It receives timing signals from the Master Clock and processes them to form timing and control signals needed to operate the MASTER Modules. The VTM sends the processed signals onto the backplane of the VME Readout Crate, where they are received by the MASTER Modules and by the VME Processor.

The VTM also contains an interface to a Global Positioning System (GPS) Receiver. The GPS time will be used to synchronize the spill period in the Near and Far Detectors. Time words are sent from the GPS Receiver on a periodic basis. The VTM receives the GPS time words and latches them to record the time of a spill using signals from the Master Clock. The GPS information can then be read out as part of the data acquisition operation, to include absolute time information along with the data from the spill.

- **The MINDER Timing Module (MTM)**

A MINDER Timing Module resides in each Front End Crate. It receives signals from the Master clock and sends them to the MINDER boards in the crate.

A description of the conceptual design of the entire clock system is given in [2].

2. Description of the Primary Timing Signals

The following is a description of the primary timing signals used by the front end electronics:

2.1. QIE Clock (QCLK)

The Master Clock provides QCLK to both the VME Readout Crate and the Front End Crate. It operates at a frequency of 53.104 MHz (hereafter referred to as 53 MHz), which is also the frequency of operation in the Fermilab Main Injector and associated beamlines. In the Front End Crates, it provides the following functions: it is used for clocking the QIEs, to integrate charge from the photodetectors; it is used for forming timestamps on the data; and it is used at half the frequency to transfer data from the MINDER Modules to the MASTER Module. In the VME Readout Crate, the MASTER Modules use the signal at half the frequency to process the data.

The signals from single photoelectrons from the photodetectors are very fast, having ~2 nS edges and ~4 nS full-width half-max widths. It is important for MINOS to be capable of accurately measuring single photoelectron signals. The QIE functions best when the charge signal is completely contained in a single clock cycle. Given that the time of flight of particles through the detector is of order 50 nS, it is desirable to have the ability to tune the QIE clock delivered to the Front End Crates to optimize the charge collection. This is accomplished by providing the ability to adjust the phase of QCLK with respect to the Main Injector RF for each Front End Crate. The adjustment shall be implemented by the Master Clock at the fan-out level. The adjustment range shall be up to one RF clock cycle, in 1 nSec steps. In addition, it is desirable to have the ability to change the overall phase of QCLK with respect to the Main Injector RF. This adjustment shall be implemented on a global basis (one adjustment for the entire system.) The adjustment shall be programmable, and have a range up to one clock cycle, with a step size of 1 nS.

In the operation of MINOS, it may be desirable to use a clock that is not in phase with the Main Injector RF, and perhaps running at a slightly different frequency. The detector has certain features that may randomize the signals relative to the Main Injector RF structure. These include: position along the scintillating fibers; propagation time in the scintillating fibers and wavelength-shifting fluors; and fluor decay time. Due to these factors, it may be desirable not to lock the phase of the clock used by the QIEs to the Main Injector RF. To accomplish this, the Master Clock shall have an on-board 53 MHz clock that operates out of phase and at a slightly different frequency from the Main Injector. The choice of which frequency source to use is an option for the experiment. In addition, the internal clock may be used for test stands, and other applications outside of the Main Injector environment.

2.2. Spill Gate (SGATE)

The Master Clock provides SGATE to the front end instrumentation in the Front End Crates, indicating when a spill occurs. This is used to configure a special state in the front end electronics, for acquiring data from the spill. The Spill Gate is derived from signals received from the Main Injector Control System. Spill Gate is used in both Single-Turn Extraction and Resonant Extraction modes.

Spill Gate must occur between 200 nSec and 1 uSec in advance of the actual spill, so that the front ends can initialize properly. Spill Gate must remain asserted while the spill is in progress, and must be de-asserted between 200 nSec and 1 uSec after the spill. This effectively forms a gate around the spill, so that the electronics can record data from every RF clock cycle in the spill.

It is desirable that there be a fixed phase relationship between SGATE and QCLK. Because QCLK can be delayed at both the global level and at the fan-out level, it is desirable to have the phase of SGATE track the phase of QCLK. As the phase of QCLK in a particular detector element is adjusted with respect to the Main Injector RF at both the global and fan-out levels, SGATE shall move with it, maintaining a constant phase relationship with QCLK. In addition, in order to accommodate a time-of-flight adjustment through the detector, an additional adjustment of SGATE is needed in the Master Clock. This adjustment shall provide a delay of SGATE in discrete units, up to 7 QCLK clock cycles (3 bits), at the fan-out level.

Because the Spill Gate signal is used in conjunction with timestamps, SGATE must be a precision signal. The signal cables must be timed uniformly to within 1 QCLK clock cycle over the entire system.

It is desirable to have the capability for Master Clock to generate an internal Spill Gate, in the event that the signals from the Main Injector are unavailable. This will be useful in test stands, and in tests on the detector. The internally generated signal can be periodic, with a period of ~2 Sec. The signal should mimic the Spill Gate signal from the signal from the Main Injector Control System in all other aspects.

2.3. Counter Reset (CNTRST)

The Master Clock provides CNTRST to the instrumentation in the Front End Crates, where it is used to reset the counters on the MINDER Modules that form the timestamps. The counters are zeroed by this signal, and then advanced with subsequent clocks.

CNTRST must occur periodically. It may be implemented using one of two techniques: arranged so that it occurs every N QIE Clocks (phased to QCLK); or arranged so that it occurs periodically (using another timing source.) If the latter technique is used, then there should be registration circuitry to align it in phase with QCLK.

The time interval should be programmable. The maximum period shall be ~2.5 seconds (1.3E8 QIE Clocks), and the minimum period shall be ~0.1 seconds (~5E6 QIE Clocks.) This gives approximately 5 bits of dynamic range, with a step size of ~0.1 seconds.

It is desirable to prevent the timestamp counters from being reset during a spill, so that there is no discontinuity of timestamps in the data record for the spill. This could happen unless special precautions are implemented, since the spills do not occur exactly periodically in time. The Master Clock must delay the generation of CNTRST if the normal timing of it occurs while SGATE is active. In that case, the Master Clock shall hold off the generation of CNTRST until after the spill. See Section 2.6 for a discussion of the hold-off conditions. CNTRST may be issued promptly if it would have occurred while SGATE is not active.

There is a similar concern about CNTRST being generated during the acquisition of cosmic ray data. Circuitry on the MINDER Modules shall prevent cosmic ray data from being acquired on the clock cycle when CNTRST is generated. The issuance of CNTRST shall have precedence in this case.

CNTRST shall be asserted for one entire clock period (19 nS), and then de-asserted. As with SGATE, it is desirable that CNTRST have a fixed phase relationship with respect to QCLK. Because QCLK can be delayed at both the global level and at the fan-out level, it is desirable to have the phase of CNTRST track the phase of QCLK. As the phase of QCLK in a particular detector element is adjusted with respect to the Main Injector RF at both the global and fan-out levels, CNTRST shall move with it, maintaining a constant phase relationship with QCLK. To accommodate a time-of-flight adjustment through the detector, an additional adjustment of CNTRST is needed. This adjustment shall provide a delay of CNTRST in discrete units, up to 7 QCLK clock cycles (3 bits), at the fan-out level.

Because the Counter Reset signal is used in the generation of timestamps, CNTRST must be a precision signal. The signal cables must be timed uniformly to within 1 QCLK clock cycle over the entire system.

2.4. Time Block Marker (TBMKR)

The Master Clock provides TBMKR to the VME Readout Crates, where it is used to form Time Blocks of data. A Time Block is defined as the data set that is collected in a certain period of time, having a common beginning time and a common ending time for all elements of the detector. There are two Readout Buffers on each MASTER Module. While data is being written into one, the VME Processor has access to the data in the other. When the Time Block Marker is received in the VME Readout Crate, the VTM generates VME Interrupt Requests that cause the buffers on the MASTER Modules to switch state: one goes from reading to writing, and the other goes from writing to reading. This creates blocks of data that are framed in time over the detector, and aids in forming triggers and reconstructing events in the DAQ System. The VME Interrupt Requests generated by TBMKR are also used to signal the VME Processor that it is time to read out a new buffer.

TBMKR must occur at regular intervals in time. As with CNTRST, it may be implemented using one of two techniques: arranged so that it occurs every N QIE Clocks (phased to QCLK); or arranged so that it occurs periodically in time (using another timing source.) As with CNTRST, if the latter technique is used, then there should be registration circuitry to align it in phase with QCLK.

The time interval for TBMKR shall be programmable. The maximum period shall be 255 mSec ($\sim 1.35E7$ QIE Clocks), and the minimum period shall be 1 mSec ($\sim 5.3E4$ QIE Clocks.) This gives approximately 8 bits of dynamic range, with a step size of 1 mSec seconds.

It is desirable to have all of the data from a spill be written to a single Readout Buffer after it has been transferred to the MASTER Module and processed. When the MASTER Module receives data from a spill, those words that are over threshold are written to the selected Readout Buffer. It is desirable to prevent the buffers from changing state while the processing of data is in progress. The interval in which data is being transferred and processed is called the *Transfer Time*. It is approximately 500 uSec long (for Single-Turn Extraction.) The Master Clock must delay the generation of TBMKR if the normal timing of it occurs while the Transfer Time is active. In that case, the Master Clock shall delay the generation of TBMKR until after the Transfer Time. See Section 2.6 for a discussion of the hold-off conditions. TBMKR may be issued promptly if it would have occurred while TBMKR is not active.

There is a similar concern about TBMKR being generated during the processing of cosmic ray data. Circuitry on the MASTER Modules shall prevent the changing of the Readout Buffer state while cosmic ray data from being processed. The DAQ System will overlap events from adjacent time blocks to take care of cosmic ray events that might fall in different time blocks in different parts of the detector.

In the rare case where both CNTRST and TBMKR occur during the same clock cycle, the Master Clock may treat them independently; these signals do not interact with each other in the front end system.

The time structure of the TBMKR signal shall have a 50% duty cycle. It shall alternate states with every TBMKR period. This provides easy identification of the state of the readout buffers across the system.

2.5. Timing Calibration (TCAL)

The Master Clock provides TCAL to the instrumentation in the Front End Crates, where it can be used for a variety of calibration operations. Some of the uses might be: to fire a charge injection circuit; to fire the light injection system; to fire the dynode discriminators in a local Front End Crate; to fire the dynode discriminators globally over the entire detector; to perform a timing calibration of the entire system.

TCAL can be arranged to occur at regular intervals, turned on and off by Run Control. As with CNTRST, it may be implemented using one of two techniques: arranged so that it occurs every N QIE Clocks (phased to QCLK); or arranged so that it occurs periodically in time (using another timing source such as a precision oscillator.) As with CNTRST, if the latter technique is used, then there should be registration circuitry to align it in phase with QCLK.

When TCAL is enabled, the time interval for the periodic generation shall be programmable. The maximum period shall be ~3 seconds (~1.6E8 QIE Clocks), and the minimum period shall be ~1 mSec (~5.3E4 QIE Clocks.) This gives approximately 12 bits of dynamic range, with a step size resolution of 1 mSec.

As with CNTRST, it is desirable to prevent TCAL from occurring during a spill. See section 2.6 for a discussion of the hold-off conditions.

The TCAL signal shall be asserted for one entire clock period (19 nSec), and then de-asserted. As with SGATE and CNTRST, it is desirable to have the phase of TCAL track QCLK. The adjustment range and resolution for the phase are the same.

Since TCAL is to be used in the calibration of timestamps, it must be a precision signal. TCAL must be timed to within 1 QCLK clock cycle over the entire system.

2.6. Hold-Off Conditions

As described in Section 2.3, it is desirable to prevent CNTRST from occurring during the spill. If the normal timing of CNTRST does occur during a spill, then the Master Clock shall hold off the generation of CNTRST for a minimum of 1 uSec after SGATE is de-asserted. This is a minimum requirement. The same shall be implemented for TCAL.

As described in Section 2.4, it is desirable to prevent TBMKR from occurring during transfer of data from the MINDER Modules to the Master Modules. If the normal timing of TBMKR does occur during the Transfer Time, then the Master Clock shall hold off the generation of TBMKR for a minimum of 1 uSec after the Transfer Time. This is a minimum requirement.

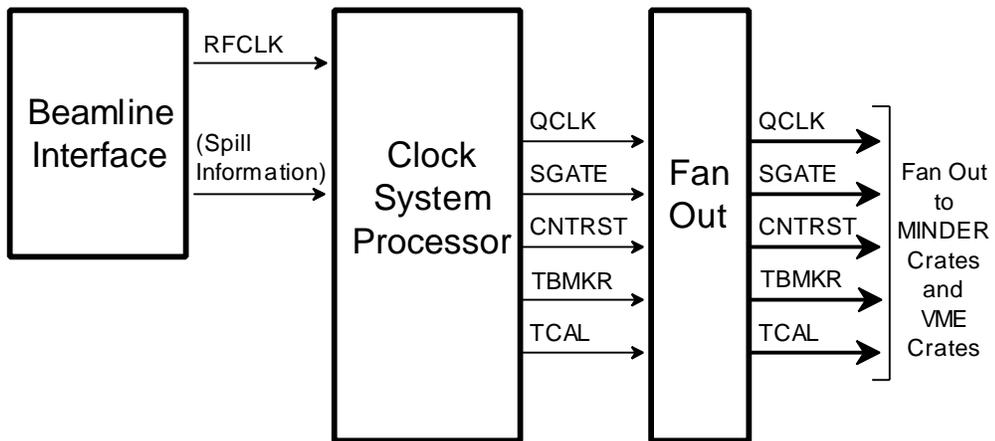
In order to reduce complexity, the three conditions described above may be combined. Define the *Hold-Off Time* as the period between the beginning of SGATE (which marks the beginning of the spill), and the end of the Transfer Time (which marks the end of the transfer of spill data to the MASTER Modules.) It is sufficient to hold off the generation of CNTRST if it occurs during the Hold-Off Time. In this case, the Master Clock shall generate CNTRST no sooner than 1 uSec but not more than 10 uSec after the Hold-Off Time is over. Likewise for TCAL, it is sufficient for the Master Clock to hold off the generation if it occurs during the Hold-Off Time. The same timing requirements apply. It is desirable for the Master Clock to prevent TCAL and CNTRST from occurring in the same clock cycle.

For TBMKR, it is sufficient to hold off the generation of the signal if it occurs during the Hold-Off Time. In this case, the Master Clock shall generate TBMKR no sooner than 1 uSec but not more than 10 uSec after the Hold-Off Time. There is no requirement in preventing TBMKR and CNTRST from occurring on the same clock cycle, as the time relationship between them is not important.

3. Technical Specifications

3.1 General Parameters

- 3.1.1 The Master Clock is the source of all of the primary timing signals described in Section 2 above.
- 3.1.2 The Master Clock components and subcomponents shall reside in a VME crate.
- 3.1.3 The Master Clock shall have a VME interface, and be capable of communicating with the VME Processor in the crate. This shall be the interface to Run Control for the experiment. The VME standard used in the MINOS experiment is VME64X.
- 3.1.4 The logical configuration for the system is shown in Fig. 2, although the physical configuration may be different. It has three subcomponents.
 - 3.1.4.1 There shall be an interface between the Master Clock and the Main Injector Control System, defined here as the Beamline Interface. This interface handles the receiving and decoding of timing information and clocks from the Main Injector Control System.
 - 3.1.4.2 The Clock System Processor receives information from the Beamline Interface, and generates the primary timing signals needed for the experiment.
 - 3.1.4.3 The primary timing signals are sent to the Clock Fan-Out, where they are distributed to the front end electronics.



* The System Contains
~50 MINDER Crates
and ~8 VME Crates.

Fig. 2 Block Diagram of Master Clock

3.1 General Parameters (Cont.)

- 3.1.5 Distribution of the primary timing signals is considered part of the Master Clock System.
- 3.1.6 Distribution of the primary timing signals from the Master Clock to the Front End Crates and the VME Readout Crates shall be done in such a way so that no significant electrical interference is received by the front end electronics as a result of the method of distribution:
 - 3.1.6.1 The clock distribution system shall not create any ground loops that include the Front End Crates nor the VME Readout Crates.
 - 3.1.6.2 The clock distribution system shall not radiate noise that causes significant interference in either the front end electronics or the photodetector electronics. The level of unacceptable interference shall be determined by the performance specifications of the front end electronics and the measurement goals of the experiment.
- 3.1.7 The distribution of clock signals shall be point-to-point connections between the fan-out and the destination crates.
- 3.1.8 The maximum length of cable in the distribution system shall not be longer than 30 meters.
- 3.1.9 All cables from the fan-out to the destination crates shall be the same lengths.
- 3.1.10 It is sufficient to have one type of fan-out that services both the Front End Crates and the VME Readout Crates, provided that all of the primary timing signals are fanned out to all of the crates.

3.2 Inputs to Master Clock

- 3.2.1 The Master Clock shall receive the 53 MHz RF (MIRF) from the Main Injector Control System. This will be one of the primary RF Reference Clocks for the system.
- 3.2.2 The Master Clock shall have an interface to the Main Injector Control System, to receive and process information about the spill (MISG). This shall be used to form the Spill Gate Reference signal.
- 3.2.3 The Master Clock may receive and process any other signals from the Main Injector Control System that are needed to achieve the performance of this specification.

3.3 Generation of QIE Clock (QCLK)

- 3.3.1 QCLK is internally generated by the Master Clock, and sent to the front end electronics as one of the primary timing signals. It is generated from the RF Reference Clock.
- 3.3.2 The Master Clock shall have an on-board 53 MHz clock source (OBRF), which can be used as the RF Reference Clock for the system.
- 3.3.3 A method shall be provided to choose the source of the RF Reference Clock, either the MIRF or the OBRF, selected through the VME interface. See Section 3.2.
- 3.3.4 QCLK shall be a periodic signal with 50% duty cycle, as delivered to the front end electronics.
- 3.3.5 The fundamental frequency shall be that of the Main Injector RF, as it occurs during the spill. The actual frequency shall be set by the Main Injector.
- 3.3.6 The rise and fall times of QCLK delivered to the front end electronics shall be 2-3 nSec.
- 3.3.7 The rising edge of QCLK, as delivered to the front end electronics, shall be referenced to the beginning of the RF cycle.
- 3.3.8 There shall be a provision to apply a global phase adjust to QCLK, in 1-2 nS steps, up to 1 clock cycle (4-5 bits), with respect to the RF Reference Clock. This shall be a programmable feature, available through the VME interface.
- 3.3.9 There shall be a provision to apply a phase adjust at the fan-out level, in 1-2 nSec Steps, up to 1 clock cycle (4-5 bits), with respect to the globally-adjusted QCLK. Each fan-out shall have an independent adjustment. This shall be a programmable feature, available through the VME interface.
- 3.3.10 The temperature stability of the phase of QCLK shall not be worse than 0.2 nSec/Degree C, as delivered to the front end electronics.
- 3.3.11 The jitter in the clock must be less than 1 nSec, as delivered to the front end electronics.
- 3.3.12 When the RF Reference Clock source is MIRF, QCLK shall be phase locked to the source during the spill, and for at least 5 uSec before and after the spill.

3.3 Generation of QIE Clock (QCLK) (Cont.)

3.3.13 When the RF Reference Clock source is MIRF, a provision shall be implemented so that the frequency of the clock does not vary by more than 1% during the time between spills, even in the presence of 1% variations in the Reference Clock.

3.4 Generation of Spill Gate (SGATE)

- 3.4.1 SGATE is internally generated by the Master Clock, and sent to the front end electronics as one of the primary timing signals. It is generated from the Spill Gate Reference signal.
- 3.4.2 The Master Clock shall have an on-board source to generate a periodic Spill Gate Reference signal (OBSG). The period shall be programmable, from 0.1 Sec to 3 Sec, in 0.1 Sec steps (5 bits.) This shall be a programmable feature, available through the VME interface.
- 3.4.3 SGATE shall be a non-periodic pulse, as delivered to the front end electronics.
- 3.4.5 The leading edge of SGATE shall occur between 200 nSec and 1 uSec before the actual spill into the detector.
- 3.4.6 The trailing edge of SGATE shall occur between 200 nSec and 1 uSec after the spill ends.
- 3.4.7 The rise and fall times of SGATE delivered to the front end electronics shall be 2-3 nSec.
- 3.4.8 SGATE shall be registered by the rising edge of QCLK at the receiving end in the front end electronics. The change in state of SGATE shall occur in enough time before the rising edge of QCLK can register the state change.
- 3.4.9 SGATE as delivered to the front end electronics shall maintain a constant phase relationship to QCLK as delivered to the same front end electronics. Any phase change of QCLK for a given fan-out shall cause there to be a corresponding phase adjustment in SGATE associated with that fan-out. See Section 3.3.8 and Section 3.3.9.
- 3.4.10 There shall be a provision to apply a delay at the fan-out level, in discrete clock cycles, up to 7 clock cycles (3 bits), with respect to the global SGATE signal. Each fan-out shall have an independent adjustment. This shall be a programmable feature, available through the VME interface.

3.5 Generation of Counter Reset (CNTRST)

- 3.5.1 CNTRST is internally generated by the Master Clock, and sent to the front end electronics as one of the primary timing signals.
- 3.5.2 CNTRST shall be a periodic pulse, as delivered to the front end electronics.
- 3.5.3 The frequency of CNTRST shall be programmable, from 0.1 Sec to 3 Sec period, in 0.1 Sec steps (5 bits). This shall be a programmable feature, available through the VME interface.
- 3.5.4 CNTRST shall have duration of 1 QCLK cycle.
- 3.5.5 The rise and fall times of CNTRST delivered to the front end electronics shall be 2-3 nSec.
- 3.5.6 CNTRST shall be registered by the rising edge of QCLK at the receiving end in the front end electronics. The change in state of CNTRST shall occur in enough time before the rising edge of QCLK can register the state change.
- 3.5.7 CNTRST as delivered to the front end electronics shall maintain a constant phase relationship to QCLK as delivered to the same front end electronics. Any phase change of QCLK for a given fan-out shall cause there to be a corresponding phase adjustment in CNTRST associated with that fan-out. See Section 3.3.8 and Section 3.3.9.
- 3.5.8 There shall be a provision to apply a delay at the fan-out level, in discrete clock cycles, up to 7 clock cycles (3 bits), with respect to the global CNTRST signal. Each fan-out shall have an independent adjustment. This shall be a programmable feature, available through the VME interface.
- 3.5.9 CNTRST must not occur during the spill, as defined when SGATE is active. The Master Clock must hold off the generation of CNTRST until after this period, for a minimum of 1 uSec after SGATE is de-asserted. See Section 2.6.

3.6 Generation of TCAL

- 3.6.1 TCAL is internally generated by the Master Clock, and sent to the front end electronics as one of the primary timing signals. It is generated from the TCAL Reference signal.
- 3.6.2 The Master Clock shall have an on-board source to generate a periodic TCAL Reference signal (OBTCAL). The period shall be programmable, from 1 mSec to 4 Sec, in 1m Sec steps (12 bits.) This shall be a programmable feature, available through the VME interface.
- 3.6.3 TCAL shall be a periodic pulse, as delivered to the front end electronics.
- 3.6.4 TCAL shall have duration of 1 QCLK cycle.
- 3.6.5 The rise and fall times of TCAL delivered to the front end electronics shall be 2-3 nSec.
- 3.6.6 TCAL shall be registered by the rising edge of QCLK at the receiving end in the front end electronics. The change in state of TCAL shall occur in enough time before the rising edge of QCLK can register the state change.
- 3.6.7 TCAL as delivered to the front end electronics shall maintain a constant phase relationship to QCLK as delivered to the same front end electronics. Any phase change of QCLK for a given fan-out shall cause there to be a corresponding phase adjustment in TCAL associated with that fan-out. See Section 3.3.8 and Section 3.3.9.
- 3.6.8 There shall be a provision to apply a delay at the fan-out level, in discrete clock cycles, up to 7 clock cycles (3 bits), with respect to the global TCAL signal. Each fan-out shall have an independent adjustment. This shall be a programmable feature, available through the VME interface.
- 3.6.9 TCAL must not occur during the spill, as defined when SGATE is active. The Master Clock must hold off the generation of TCAL until after this period, for a minimum of 1 uSec after SGATE is de-asserted. See Section 2.6.

3.7 Generation of Time Block Marker (TBMKR)

- 3.7.1 TBMKR is internally generated by the Master Clock, and sent to the front end electronics as one of the primary timing signals.
- 3.7.2 TBMKR shall be a periodic signal with a 50% duty cycle, as delivered to the front end electronics.
- 3.7.3 The frequency of TBMKR shall be programmable, from 1 mSec to 255 mSec period, in 1 mSec steps (8 bits). This shall be a programmable feature, available through the VME interface.
- 3.7.4 The rise and fall times of TBMKR as delivered to the front end electronics shall be 2-3 nSec.
- 3.7.5 TBMKR shall be registered by the rising edge of QCLK at the receiving end in the front end electronics. The change in state of TBMKR shall occur in enough time before the rising edge of QCLK can register the state change.
- 3.7.6 TBMKR as delivered to the front end electronics shall maintain a constant phase relationship to QCLK as delivered to the same front end electronics. Any phase change of QCLK for a given fan-out shall cause there to be a corresponding phase adjustment in TBMKR associated with that fan-out. See Section 3.3.8 and Section 3.3.9.
- 3.7.7 TBMKR must not occur during the transfer and processing of data from the MINDER Modules to the MASTER Modules (approximately 500 uSec.) The Master Clock must hold off the generation of TBMKR until after this period, for a minimum of 1 uSec after the transfer and processing of data is completed. See Section 2.6.

4. Bibliography

- [1] G. Drake, J. Dawson, C. Nelson, "Overview of the Front End Electronics for the MINOS Near Detector," NUMI Internal Note 628, Version 1.35, Nov. 15, 1999.
- [2] J. Dawson, G. Drake, C. Nelson, C. Perry, A. Weber, "Conceptual Design of the Clock System for the MINOS Near Detector," NUMI Internal Note 626, Version 2.1, July 25, 2000.