

**Fermi National Accelerator Laboratory**

**Particle Physics Division  
Engineering and Technical Teams Department**

**MINOS  
Master Clock System  
Preliminary Design Specification**

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## 1. Introduction

The Minos Master Clock's main function is to distribute QIECLK to the front-end electronics with precision control, low drift, and low jitter. The timing signals SGATE, CNTRST, TBMKR, and TCAL are also generated and distributed to the front-end electronics with a fixed phase relationship to QIECLK. The Master Clock system consists of several parts:

The Master Clock VME Crate is at the top level of hierarchy and contains one Master Clock Control (MCC) module, Four Master Clock Fanout (MCF) modules, and a VME processor. The Master Clock Control Module interfaces to the Main Injector via connections to the Link Repeater and Camac 479 module. The MCC provides the Master Reference QIECLK and associated timing signals. The MCC also contains a VME slave interface for communication with the VME processor.

The Master Clock Fanout modules (MCF) distribute clock and timing to fifty front end crates and eight VME crates via high speed serial transmitters. The serial link provides a fixed phase relationship between QCLK and timing signals to the front ends while still allowing QCLK phase adjustment. An LVDS-B slow control link is also implemented for each front end connection to download delay information, monitor HOTLink lock status, initiate tests, etc. The MCF modules also have a VME slave interface for parameter download, phase offset adjustments, slow control commands, etc.

Each Front End Crate contains a Minder Timing Module (MTM). The MTM receives and decodes clock and timing information from the MCF and fans out this information to sixteen Minder modules within the crate via front panel connections. A slow control link is also implemented on the MTM for receiving delay information from the MCF and sending status, etc. There are 50 MTM modules in the system.

Each VME Master crate contains a VME Timing Module (VTM). The VTM decodes clock and timing information and fans out a 26.5 MHz clock via the backplane to each VME Master module. It also has a VME slave interface to pass along time stamp information to the VME Computer. One VTM contains a GPS interface to time stamp data in real time for later comparison with the Minos far detector data.

# MINOS Master Clock System Block Diagram

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58 Serial Link Outputs (for Clock and control)  
and 58 slow control bi-directional connections to Front  
End Minder and VME Crates over single cable per crate;  
16 front panel RJ45 connectors per MCF module

Front Panel (point to point) Clock and Timing fanout from MTM to  
16 Minder Modules via front panel RJ45 Jacks and Cat 5e/6cable

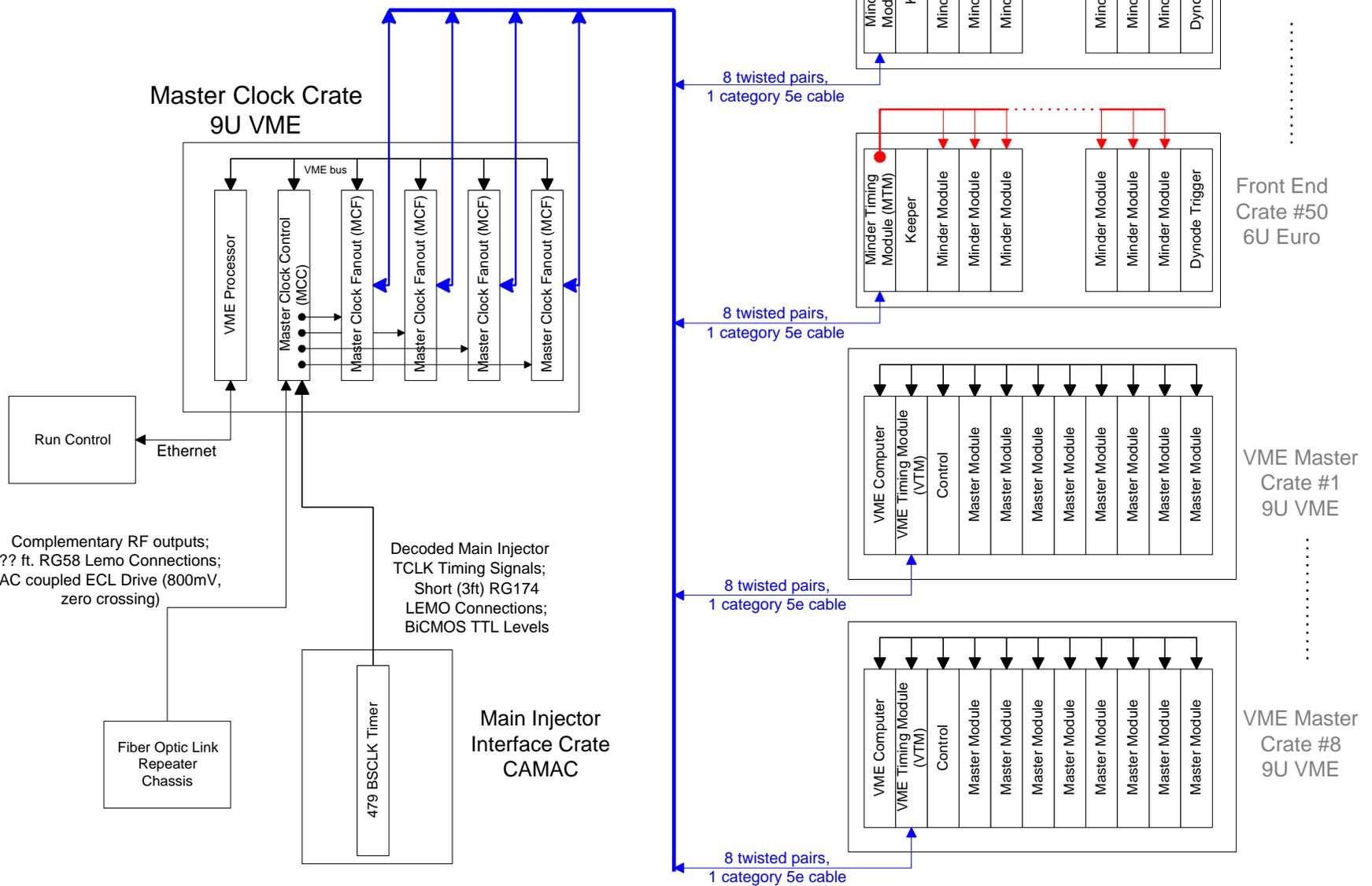


Figure 1-1 MINOS Master Clock System

## 2. Master Clock Controller (MCC)

The Master Clock Controller (MCC) is the top level clock and timing module for the MINOS near detector. Interface to the Main Injector is included on this module with connections to the Link Repeater chassis (RF) and a CAMAC 479 module (Beam timing signals). A VME Interface is included for parameter setup, timing signal rate settings, delays, etc. The clock and timing signal outputs of the MCC are driven on the backplane to four Master Clock Fanout (MCF) modules.

### 2.1. Main Injector Interface

The Main Injector (MI) timing signals that will be distributed to MINOS include the 53 MHz low-level RF, TCLK, and the MIBS clock all of which are transported to MINOS via fiber optic cable. Although the low level RF will be coherent to the beam during flat top and during the spill, at other times it will vary significantly (10% or more). TCLK is a 10 MHz encode clock that distributes the timing of various Main Injector events in real time but is not itself synchronous to the beam. The MIBS clock is synchronous to beam in the Main Injector and runs at 7.5 MHz (RF/7) and is encoded with bucket level timing events. The Controls Group of the Beams Division will provide hardware and support to interface with and decode Main Injector timing. The RF reference for the Master Clock is provided from the Link Repeater via a front panel Lemo connector. An 800mV zero referenced 53MHz signal is generated with a rise time of 2nS and a jitter specification of 600ps peak to peak. MIBS control signals are derived from the CAMAC 479 BSCLK Timer. Four user programmable outputs (EPROM based) are available using BCT (BiCMOS TTL compatible) drivers. The CAMAC crate and VME crate housing the Master Clock are expected to be in the same relay rack.

### 2.2. Long-term Timing Drift

The long-term phase drift of the low-level RF with time and temperature relative to the beam at the MINOS detector needs to be determined. A study of the long-term drift of accelerator timing signals at D0 relative to the beam is presented in Ref [1]. The study showed a long-term drift of accelerator timing signals derived from the TVBS clock distributed using copper cables over a distance of approximately 14,000 feet to be 15.6ns. The same study showed a long-term drift of the same signals derived from the APTVBS clock distributed using optical fiber cables over a distance of 7000 feet to be 8 ns. In the same study, the long-term drift of the low level RF distributed over the Fermilab CATV system to be 1.2 ns. The study did not determine the source of the drift.

The distance from the Main Injector to the MINOS detector is approximately 4100 feet and it is expected that timing signals including the low level RF are to be distributed over fiber optic cable. Hence, the stability of these signals at the Minos detector needs to be understood. If the signals do drift, it may be possible to apply the feedback techniques discussed in Ref [2] to provide stable timing signals at MINOS. An alternate but less desirable approach would be to measure the RF phase drift relative to the beam and manually adjust the phase the RF as necessary.

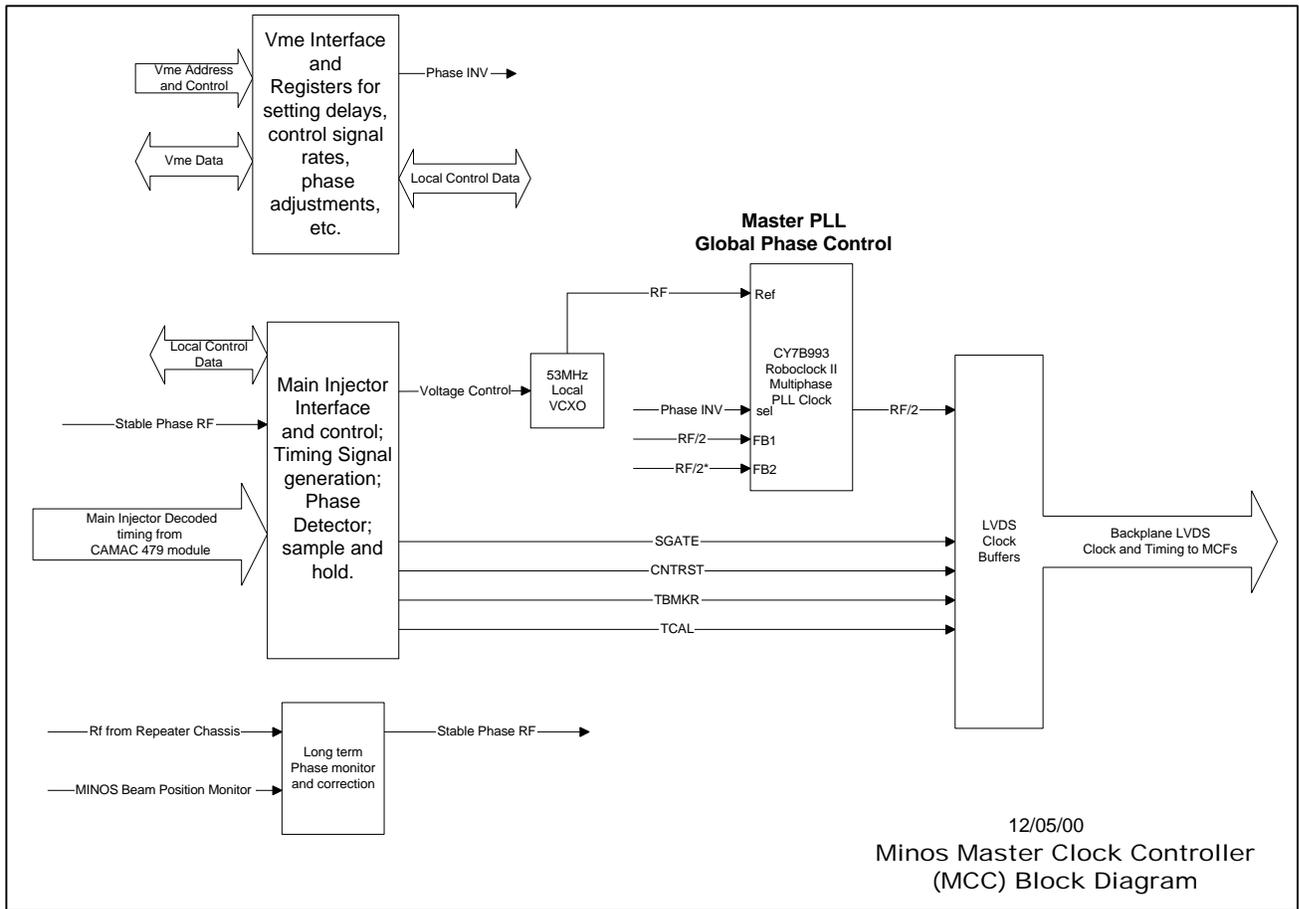
### 2.3. RF Frequency Variation and Compensation

The Main Injector RF frequency changes while ramping from 8GeV to 120GeV, rapidly changes after extraction, flat tops at different frequencies (energies) for various other non-NuMI cycles, and glitches while resynchronizing the booster, etc. Hence, to provide a stable clock to the MINOS front-end electronics, a 53.1047MHz voltage controlled oscillator (VCXO) has been chosen as the main clock source. Greater than 90% of the time the VCXO will be free running, providing a very stable uninterrupted QIECLK very close in frequency to the Main Injector flat top frequency (within <25ppm). The CAMAC 479 module can be programmed to detect NuMI cycles (TCLK event \$23) and flat top (TCLK event \$25). These signals are passed along to the Master Clock (possibly delayed) to indicate that the Main Injector is stable at flat top (53.1MHz). At this time the Master Clock enables a sample and hold amplifier connected to the output of a phase detector that compares the VCXO RF with the Main Injector RF. The phase detector applies the appropriate correction to the voltage control of the VCXO and the phase is slowly changed (Max rate 15KHz) until it is locked to the incoming Main Injector RF. After the extraction (TCLK event \$26), the sample and hold switch opens and the VCXO "remembers" the flat top frequency until the next NuMI flat top. Using the sample and hold method ensures that the VCXO frequency stays very close to the Main Injector frequency, allowing for minimum lock times at the next flat top. Lock time is estimated to be < 100uS.

Second order effects from the sample and hold circuit are expected to be very minimal. Using a very low droop sample and hold amplifier such as the Analog Devices SMP04, droop effect over 10 seconds would cause a VCXO frequency change of about 25 Hz. Charge injection effects when opening the switch are estimated to cause even less frequency shift (<25 Hz).

**2.4. MCC Timing Signal Generation**

Kicker event (TCLK event \$A9 or MIBS event \$74) along with a programmable delay establish when the kicker fires to transfer protons from the Main Injector to NuMI. The Master Clock would use one of these signals along with a revolution marker on MIBS clock to generate SGATE. Programmable timers in the Master Clock would generate the periodic signals CNTRST, TBMKR, and TCAL. These signals would not occur during SGATE or subsequent data transfer from the MTMs to the VTMs. Internal gating is provided to meet the hold-off requirements for each of these signals. In a local mode, SGATE can be provided under VME processor control or via a programmable, periodic setting. Global phase control of QCLK is programmable in 8 steps of 1.17nS in the Roboclock II PLL over the range of 1/2 QCLK cycle (9.4nS). In conjunction with a phase inversion, the effective control range of QCLK becomes 18.8ns. The period of the REFCLK is multiplied by 2 in the Roboclock to generate a 26.5MHz output frequency. Clock (QCLK/2) and timing signals are bussed to the Master Control Fanout (MCF) modules using an LVDS common bus multi-drop configuration.



**Figure 2-1 Master Clock Controller (MCC) Block Diagram**

### 3. Master Clock Fanout (MCF)

The Master Clock Fanout (MCF) receives clock and timing signals from the MCC and distributes them to up to 16 MTM/VTM modules. A VME Interface is included to download delays, communicate with the front ends via the slow control interface, set up and reframe HOTLink serial links, and perform diagnostic tests.

#### 3.1. MCF QCLK Adjustment and Fanout

An array of 8 Cypress Roboclock II multiphase PLL clock drivers (Fanout PLLs) receive the converted LVDS signals from the MCC. Two output banks of each Fanout PLL provide individual fine delay adjustments of the QCLK. 8 steps of 1.17nS are possible with the 26.5 MHz reference frequency. This 9.4nS delay range accounts for one half of a QIECLK period. To achieve a full 18.8nS (one period) fine tuning range the QCLK can be inverted at the MTM PLL clock buffer.. The delayed and divided frequency is used as the reference source for the Cypress HOTLink based serial clock transmission system.

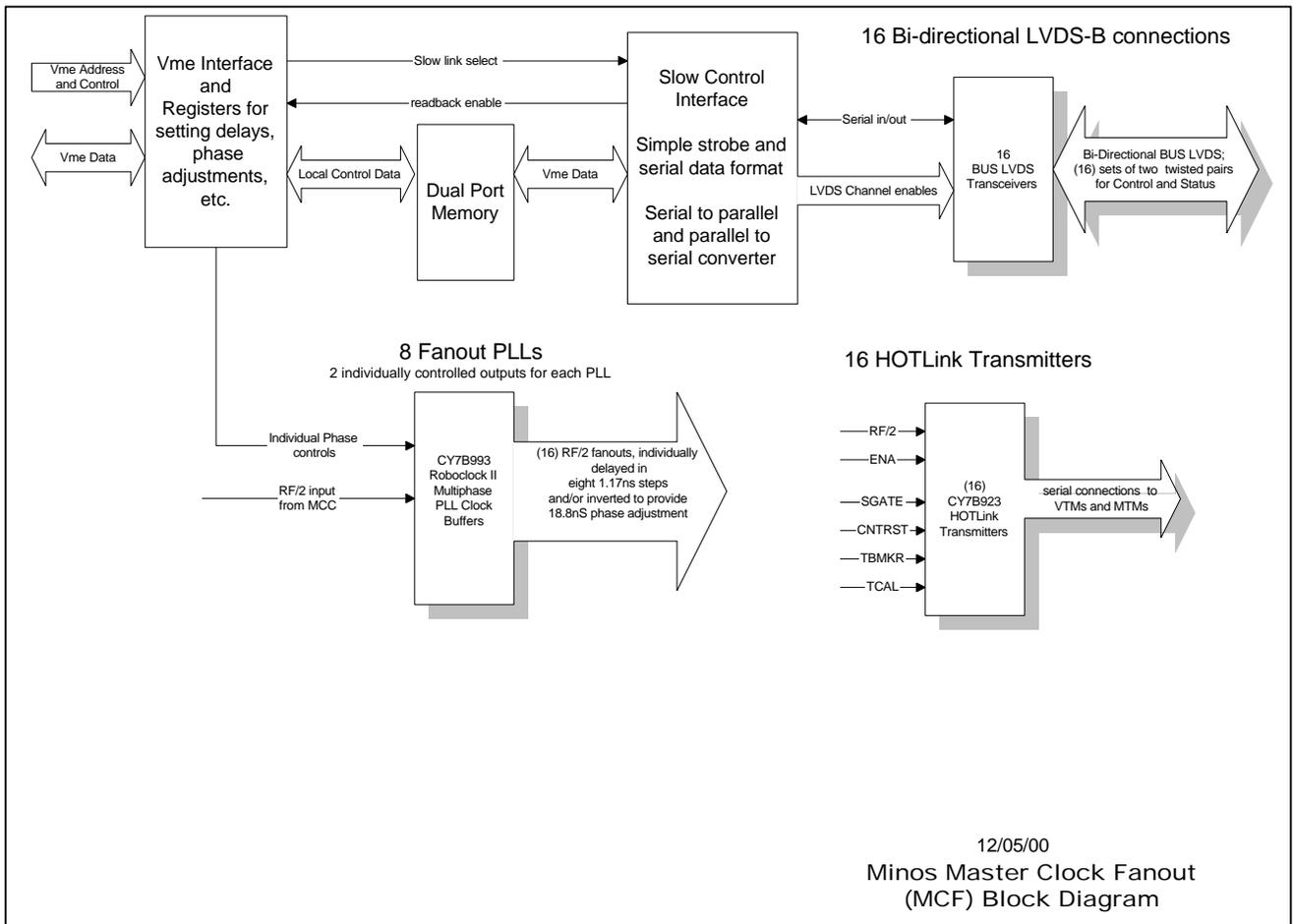


Figure 3-1 Master Clock Fanout (MCF) Block Diagram

#### 3.2. HOTLink Serial Transmission

The HOTLink chipset consists of a CY7B923 transmitter and a CY7B933 receiver. The 26.5MHz reference is in the middle of the chipset's operating range. Eight bits of data are serialized using an 8b/10b encoding scheme for a serialized bandwidth of 265 Mbits/sec. The input data for the transmitter are the SGATE, CNTRST, TBMKR, and TCAL signals. Using this method these four (and any others, as there are 8 bits available) signals maintain a fixed phase relationship to the QIECLK from the Master Clock to the MTM/VTM. Greater than 99% of the time, the HOTLink chipsets will be running an idle K28.5 test pattern.

When a timing signal is to be distributed to the front ends, the HOTLinks are enabled for one 26.5MHz clock period and the appropriate timing signal is fanned out to all bit x inputs of the HOTLink transmitters. The generation of timing signals is expected to occur at the falling edge of the 26.5MHz clock to meet setup and hold parameters for all HOTLink reference clocks, since delay of up to 9.4nS is possible.

### **3.3. MCF Slow Control Interface**

A series of slow control interface links between the Master Clock and MTM/VTM modules is envisioned for parameter download and readback, HOTLink lock status, errors, etc. A simple bi-directional strobe and serial data protocol using 2 pairs of the network cable is planned. BUS LVDS is a logical choice for transmission technology, having been designed for high speed bi-directional bus applications. It is expected that the slow speed chosen for this link (1Mbit/sec?) will make its design and operation relatively easy, avoiding charged cable concerns and the need for cable equalization. The simple strobe and data format eliminates crosstalk within the cable since the HOTLink driven clock is the only active pair during data taking. The Master Clock and each MTM/VTM will have a slow control interface PLD that serializes outgoing data and deserializes incoming data. On the Master Clock, a Dual Port Memory holds the parameter download information to be sent to the front end modules. Parameters may include delay information for timing signals, clock inversion, link test data, etc. Parameters are sequenced to each front end modules under VME control. A portion of the Dual Port Memory is also used for parameter and status readback. The interface on the MTM/VTM is similar, but the commands are always initiated from the Master Clock. With only a few parameters and status objects to be stored, registers within the MTM/VTM slow control interface PLD are sufficient (no need for a Dual Port Memory).

### **3.4. Fanout Connections and Cables**

The physical connection between the Master Clock crate and the MTM/VTM modules is expected to be one Category 5e or Category 6 network cable for each Master to MTM/VTM connection. The termination of the cable is a high performance RJ45 connector on both ends. The standard network cable consists of 4 unshielded, twisted pairs. One pair is to be used for Clock fanout via the HOTLink chipset. Two other pairs are to be used for a slow control interface. An unused pair is available for expansion or can be used if a ground reference is desirable.

### 4. Minder Timing Module (MTM)

The Minder Timing Module's (MTM) main function is to recover clock and timing signals from the serial link and distribute them with precision timing (~1nS skew) to the 16 Minder Modules in the front end crate. The MTM is situated in the front end 6U Eurocrate, using only power and ground pins from the backplane. There is no VME interface in this crate.

#### 4.1. HOTLink Receiver and Timing Signal Recovery

At the receiving end of the HOTLink set on the MTM, the receiver locks on to the incoming stream of data using its own reference clock. This reference clock is provided by a precision oscillator that must be within 0.1% of the incoming bit stream. A 26.5MHz (RF/2) output clock from the HOTLink receiver is provided for the 8 bit parallel data stream. The 26.5MHz clock is fed to a PLL buffer where the frequency is multiplied by 2 to recover the QIECLK. The 8 bit data stream is monitored by logic that decodes a valid byte of data into the appropriate timing signal (SGATE, CNTRST, TBLMKR, and/or TCAL).

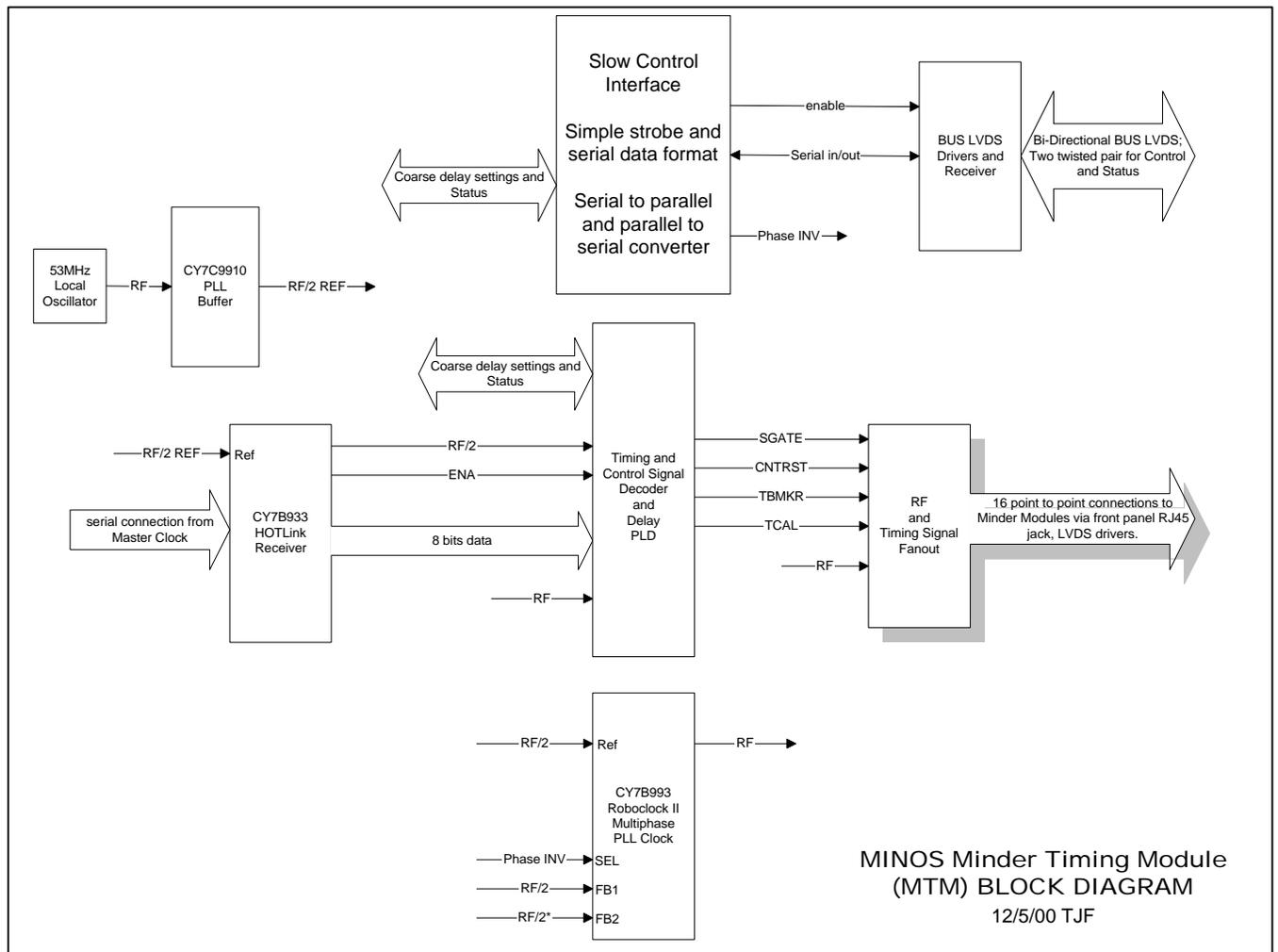


Figure 4-1 Minder Timing Module (MTM) Block Diagram

**4.2. Clock and Timing Delay and Distribution**

Coarse delay of the timing signals in QCLK (18.8nS) steps is accomplished by preloading a counter for each signal with the desired number of RF steps using the slow control link. A 4 bit counter allows 16 delay steps for each timing signal. The appropriately delayed signals are distributed to 16 LVDS fanout driver sets, one for each Minder Module. The signals are to be distributed via front panel point to point connections using matched length twisted pair cables. The QCLK (and timing signals) can be inverted via the slow control interface, completing the 18.8nS fine delay range of the QCLK (QCLK is delayed in 8 steps of 1.17nS on the MCF modules).

**4.3. MTM Slow Control Interface**

The MTM slow control interface is similar in design to the MCF slow control interface, using a simple strobe and serial data protocol. All read and write commands originate from the MCF via the VME Processor. Delay registers can be set and read back, HOTLink and other types of status can also be latched and read back to the Master Clock.

### 5. VME Timing Module (VTM)

The VME Timing Module (VTM) recovers clock and timing information from the serial link and fans out a 26.5MHz clock and TBMKR to all VME Master modules in the crate. It also latches certain timing information for inclusion in the data record. A GPS Interface is also included.

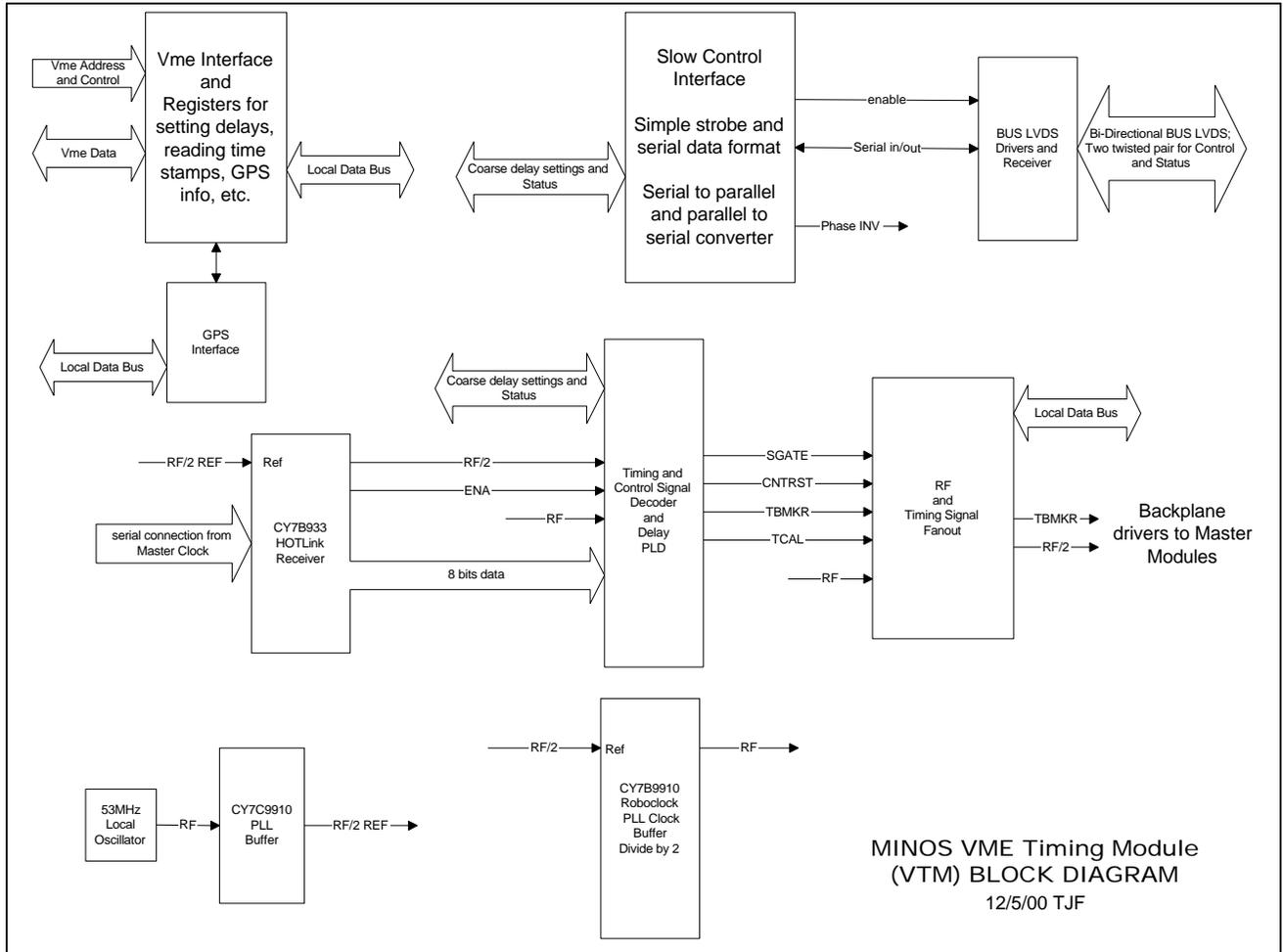


Figure 5-1 VME Timing Module (VTM) Block Diagram

#### 5.1. Clock/Timing Recovery and Fanout

Clock and timing are recovered by the VTM in much the same way as is done on the MTM. The 26.5MHz clock and the decoded TBMKR are fanned out to Master modules on the VME backplane. The backplane skew is not an issue as these signals are not precision timing signals for the system.

#### 5.2. VME Interface

The VTM has a simple VME slave interface to read out time stamp, GPS, status, and other information.

### 5.3. VTM Slow Control Interface

The VTM slow control interface is very similar to the MTM interface. There are some registers and settings that will not be applicable to the operation of the VTM. However, the logic and protocol will be kept the same for software and MCF hardware simplicity.

### 5.4. GPS Interface

One VTM contains a GPS Interface to help mark events in real time, to later be correlated with data from the far detector. It is intended that the GPS detection circuitry be a simple, commercially available chipset or module/daughter card.

## 6. Global Initialization and Testing

The Master Clock System must have an initialization procedure resident in the Master Clock VME Processor. Run Control should be able to start the procedure via Ethernet connection to the VME Processor. Serial links must be "reframed", delays downloaded and checked, etc. before a run can begin. Global testing should be provided in a stand alone mode where the Master Clock System provides all relevant clock and timing signals, under the control of the Master Clock VME processor or in a free running mode. It may also be desirable to have a local front end crate test mode where the MTM is able to provide clock and timing locally for the Minder modules.

## 7. Self Test Features

The Master Clock system will have some test features implemented to validate and test the HOTLink connections and the slow control link. All parameters and operating conditions used in the front end crates will be available for monitoring purposes via the slow control link. The HOTLink chipset has a BIST mode (Built In Self Test) for testing the integrity of the high speed data links. Other simple programs will be developed for checking the transmission of actual data on the high and low speed links.

## 8. References

- 1) S. Chappa, "Long-term Stability of the TVBS and APTVBS Signals, D0 Note #3537, July 2, 1993.
- 2) W. Blockland and J. Steimel, "Main Injector Synchronous Timing System", Fermilab-Conf-98/165, February 1999.

