

MCC VME MAP

Address	Function	valid	read/	Function
24 bit HEX	Name	data	write	Description
0x100000	CSR0	D[7..0]	R/W	General purpose control status, currently not defined
0x108000	CLK_CNTRL[31..16]	D[15..0]	R	Roboclock control settings, diagnostic only
0x110000	CLK_CNTRL[15..0]	D[15..0]	R	Roboclock control settings, diagnostic only
0x118000	CLK_CNTRL_OE[31..16]	D[15..0]	R	Roboclock control settings, diagnostic only
0x120000	CLK_CNTRL_OE[15..0]	D[15..0]	R	Roboclock control settings, diagnostic only
0x128000	GLOBAL_PHASE[4..0]	D[4..0]	R/W	Global Phase Adjustment, 24 steps of 785pS
0x180000	SGATE ONE SHOT	N/A	W	Each write generates one SGATE
0x188000	CNTRST ONE SHOT	N/A	W	Each write generates one CNTRST
0x190000	TCAL ONE SHOT	N/A	W	Each write generates one TCAL
0x198000	TBMKR ONE SHOT	N/A	W	Each write generates one TBMKR
0x1A0000	TIMING 4 ONE SHOT	N/A	W	Spare timing signal 4 one shot
0x1A8000	TIMING 5 ONE SHOT	N/A	W	Spare timing signal 5 one shot
0x1B0000	TIMING 6 ONE SHOT	N/A	W	Spare timing signal 6 one shot
0x1B8000	TIMING 7 ONE SHOT	N/A	W	Spare timing signal 7 one shot
0x1C0000	CSR1	D[7..0]	R/W	Main control register for timing signal control
0x1C8000	SGATE_DEL[7..0]	D[7..0]	R/W	SGATE delay from MIBS74 in MIBSAA steps
0x1D0000	SGATE_DUR[8..0]	D[8..0]	R/W	SGATE duration in steps of 37.6nS
0x1D8000	LOC_SGATE_PER[7..0]	D[7..0]	R/W	Local SGATE period in steps of 19.7mS
0x1E0000	CNTRST_PER[7..0]	D[7..0]	R/W	CNTRST period in steps of 19.7mS
0x1E8000	TCAL_PER[15..0]	D[15..0]	R/W	TCAL period in steps of 154uS
0x1F0000	TBMKR_PER[8..0]	D[8..0]	R/W	TBMKR period in steps of 616uS
0x1F8000	LOCK_CHECK[11..0]	D[11..0]	R/W	Trigger signal for testing lock time, diagnostic only

Colin/Tim, above is the general memory map of the MCC. For CALDET, only a few of these functions will be utilized. The MCC is an A24, D16 slave. It will respond to A32/D32 commands, but try to avoid D8 read/writes. The most important register is the Control/Status Register "CSR1". It breaks down as follows:

CSR1 BIT	Function
0	0 = Main Injector mode (or CALDET Mode), 1 = Local Timing Mode
1	0 = Main Injector SGATE, 1 = Local SGATE periodic disabled
2	0 = CNTRST periodic enable, 1 = CNTRST periodic disabled
3	0 = TCAL periodic enabled, 1 = TCAL periodic disabled
4	0 = TBMKR periodic enabled, 1 = TBMKR periodic disabled
5	0 = CALDET 40MHz CNTRST AND TBKMR enabled, 1 = CALDET TBMKR disabled
6	Reserved
7	Reserved
8	Lock Status of main MCC Roboclock master timing, read only, 1 = locked

Upon powerup, the CALDET MCC defaults CSR1 to Hex 36. This translates to CALDET clock mode with TBMKR disabled. To start a run, just change CSR1 from \$36 to \$16. Write \$36 again to stop a run. The TBMKR will start/stop on the next PPS after the register is changed.

I have simplified the TBMKR period (buffer swap) settings to one of four selections. Normally there is a 9 bit register at 0x1F0000 that sets the TBMKR period in steps of 616uS. For CALDET, when CSR1[5] = 0, TBMKR period is a 2 bit register with TBMKR period as follows (default = 0, can be changed to suit your preference):

TBMKR REGISTER (0X1F0000) SETTINGS - 2 BITS	
0	PERIOD = 10mS
1	PERIOD = 25mS
2	PERIOD = 50mS
3	PERIOD = 100mS

I'm sure there are several details to be worked out, but this should get us going!

Cheers, Tom
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