

MCC VME MAP

Address	Function	valid	read/	Function
24 bit HEX	Name	data	write	Description
0x100000	CSR0	D[7..0]	R/W	General purpose control status, currently not defined
0x108000	CLK_CNTRL[31..16]	D[15..0]	R	Roboclock control settings, diagnostic only
0x110000	CLK_CNTRL[15..0]	D[15..0]	R	Roboclock control settings, diagnostic only
0x118000	CLK_CNTRL_OE[31..16]	D[15..0]	R	Roboclock control settings, diagnostic only
0x120000	CLK_CNTRL_OE[15..0]	D[15..0]	R	Roboclock control settings, diagnostic only
0x128000	GLOBAL_PHASE[4..0]	D[4..0]	R/W	Global Phase Adjustment, 24 steps of 785pS
0x180000	SGATE ONE SHOT	N/A	W	Each write generates one SGATE
0x188000	CNTRST ONE SHOT	N/A	W	Each write generates one CNTRST
0x190000	TCAL ONE SHOT	N/A	W	Each write generates one TCAL
0x198000	TBMKR ONE SHOT	N/A	W	Each write generates one TBMKR
0x1A0000	TIMING 4 ONE SHOT	N/A	W	Spare timing signal 4 one shot
0x1A8000	TIMING 5 ONE SHOT	N/A	W	Spare timing signal 5 one shot
0x1B0000	TIMING 6 ONE SHOT	N/A	W	Spare timing signal 6 one shot
0x1B8000	TIMING 7 ONE SHOT	N/A	W	Spare timing signal 7 one shot
0x1C0000	CSR1	D[7..0]	R/W	Main control register for timing signal control
0x1C8000	SGATE_DEL[7..0]	D[7..0]	R/W	SGATE delay from MIBS74 in MIBSAA steps
0x1D0000	SGATE_DUR[8..0]	D[8..0]	R/W	SGATE duration in steps of 37.6nS
0x1D8000	LOC_SGATE_PER[7..0]	D[7..0]	R/W	Local SGATE period in steps of 19.7mS
0x1E0000	CNTRST_PER[7..0]	D[7..0]	R/W	CNTRST period in steps of 19.7mS
0x1E8000	TCAL_PER[15..0]	D[15..0]	R/W	TCAL period in steps of 154uS
0x1F0000	TBMKR_PER[8..0]	D[8..0]	R/W	TBMKR period in steps of 616uS
0x1F8000	LOCK_CHECK[11..0]	D[11..0]	R/W	Trigger signal for testing lock time, diagnostic only