



SMD Channel Arrangement and Output Ordering

Jinyuan Wu
January 15, 1999

SMD Channel Arrangement and Output Ordering

Introduction:

This document provides information on the SMD channel assignment and output ordering. The SMD system accepts 32 or 48 channels of input signals from the detector. The digitized data are output to the SMXR board. It is required that adjacent channels are sent into SMXR in consecutive order.

The input signals are sent through an auxiliary board, SMDAUX, to the SMD board. Each SMDAUX board accepts 3 34-pin connectors and the signals are mapped onto a 96-pin connector (VME P2) linking to the SMD board.

On the SMD board, the input signals are brought to 12 SQUID cards each accepting 4 channels. The 12 SQUID cards are grouped into 4 groups. Each group sends 11 data bits to a PLD, SMDDT which selects 11 out of the 44 data bits every 33ns. The output of the PLD becomes the data flow sent to SMXR.

Therefore, the order of the data seen at SMXR board depends on the routing of SMDAUX and SMD boards and enable coding of the SQUID cards. We will discuss these aspects in the following sections.

SMDAUX routing:

The SMDAUX board links three 34-pin connectors from the detector to the 96-pin connector. The channels are mapped such that the routing on the SMD board is as designed and simple. There are 48 channels sent through the SMDAUX board, 16 on each input connector.

- The three connectors from top to bottom hold channels 00-15, 16-31 and 32-47, respectively.
- In the December 1997 version, the 17th pair of the pins are unused. While from the RABBIT design, the 1st pair was unused. The temporary fix is to cut the 1st pair of pins of the connector header and solder it on board with pins shifted up one pair.
- This will let the 1st pair of the connector to be unused and the 2nd pair to be channel 00 (or 16, or 32) and the 17th pair to be channel 15 (or 31, or 47).
- The channel assignment on the 96-pin connector are shown in the following table.

INPUT(00)	INPUT(04)	INPUT(08)
RETRN(00)	RETRN(04)	RETRN(08)
INPUT(12)	INPUT(16)	INPUT(20)
RETRN(12)	RETRN(16)	RETRN(20)
INPUT(24)	INPUT(28)	INPUT(32)
RETRN(24)	RETRN(28)	RETRN(32)
INPUT(36)	INPUT(40)	INPUT(44)
RETRN(36)	RETRN(40)	RETRN(44)
INPUT(01)	INPUT(05)	INPUT(09)
RETRN(01)	RETRN(05)	RETRN(09)
INPUT(13)	INPUT(17)	INPUT(21)
RETRN(13)	RETRN(17)	RETRN(21)
INPUT(25)	INPUT(29)	INPUT(33)
RETRN(25)	RETRN(29)	RETRN(33)
INPUT(37)	INPUT(41)	INPUT(45)
RETRN(37)	RETRN(41)	RETRN(45)
INPUT(02)	INPUT(06)	INPUT(10)
RETRN(02)	RETRN(06)	RETRN(10)
INPUT(14)	INPUT(18)	INPUT(22)
RETRN(14)	RETRN(18)	RETRN(22)
INPUT(26)	INPUT(30)	INPUT(34)
RETRN(26)	RETRN(30)	RETRN(34)
INPUT(38)	INPUT(42)	INPUT(46)
RETRN(38)	RETRN(42)	RETRN(46)
INPUT(03)	INPUT(07)	INPUT(11)
RETRN(03)	RETRN(07)	RETRN(11)
INPUT(15)	INPUT(19)	INPUT(23)
RETRN(15)	RETRN(19)	RETRN(23)
INPUT(27)	INPUT(31)	INPUT(35)
RETRN(27)	RETRN(31)	RETRN(35)
INPUT(39)	INPUT(43)	INPUT(47)
RETRN(39)	RETRN(43)	RETRN(47)

- Pin Assignment of the 96 pin Connector.

SMD input routing and SQUID grouping:

There are 12 SQUID card sockets on each SMD board. They are named as SQD1 to SQD12. Each SQUID card sockets has four input channels: BOTIN1, TOPIN1, BOTIN0 and TOPIN0. The channels assigned to them for the SQD1 to SQD12 are shown in the following table:

	TOPIN0	TOPIN1	BOTIN1	BOTIN0
SQD1	00	04	08	12
SQD2	16	20	24	28
SQD3	32	36	40	44
SQD4	01	05	09	13
SQD5	17	21	25	29
SQD6	33	37	41	45
SQD7	02	06	10	14
SQD8	18	22	26	30
SQD9	34	38	42	46
SQD10	03	07	11	15
SQD11	19	23	27	31
SQD12	35	39	43	47

The digital data output lines of every three SQUID cards are connected together and thus form 4 groups. Specifically, data output lines of SQD1, SQD2 and SQD3 are wired together and 11 bits of data are sent out from this group of SQUID cards. The SQD4, 5 and 6 form the second group and SQD7, 8 and 9 the third and SQD10, 11 and 12 the fourth. These four groups send 44 bits of data every 132ns.

- These 44 bits of data are called a “quad set”.
- A “quad set” contains data from four channels in consecutive order. The first “quad set” contains channel 00, 01, 02 and 03, the second contains 04, 05, 06 and 07, and so on.
- Data in a “quad set” are sent to SMXR board 11 bit at a time, every 33ns. They are in a sequence of consecutive order.

Each SQUID card accepts four channels of inputs. On each SQUID card, there are two SMQIE chips, one on top and the other on bottom of the card. Each SMQIE chip accepts two input channels: channel 0 and channel 1. If a SMQIE chip is selected, it puts data onto the 11 bit output data line.

- There are 6 enable lines, GRP0 to GRP5 on the SMD board. Each enables 4 SMQIE chips which will put 44 bits of data.
- A channel select signal CHSEL is attached to all the SMQIE chips. This signal determines data of which input channel should be presented on the data output.

SMQIE enable sequence:

The SMQIE chips are enabled in such a sequence that the data read out from the SMD board are in the consecutive channel order.

- In the 48 channel mode, data are read out for channel 00, 01, ..., 47. They are all from the time slice buffer 0, i.e. TS=0.
- In the 32 channel mode, data for channel 00, 01, 02 and 03 are first readout for TS=0. Then the same "quad set" are repeated for TS = 1, 2 and 3. After all the four time slices are read out, the next "quad set" for channel 04, 05, 06 and 07 is enables and the four time slices are repeated.

The following table shows the read out sequence of the first a few "quad set" in 32 channel mode.

Channel	TS
00	0
01	
02	
03	
00	1
01	
02	
03	
00	2
01	
02	
03	
00	3
01	
02	
03	
04	0
05	
06	
07	
04	1
05	
06	
07	
04	2
05	
06	
07	
04	3
05	
06	
07	

A condensed version of this table is shown in the following. The information on the enable lines and the channel selection signal is also shown.

Enable line	SQD	TOP /BOT	CHSEL	Channels			
				TS = 0	TS = 1	TS = 2	TS = 3
GRP0	1,4,7,11	TOP	0	00, 01, 02, 03	00, 01, 02, 03	00, 01, 02, 03	00, 01, 02, 03
			1	04, 05, 06, 07	04, 05, 06, 07	04, 05, 06, 07	04, 05, 06, 07
GRP1		BOT	1	08, 09, 10, 11	08, 09, 10, 11	08, 09, 10, 11	08, 09, 10, 11
			0	12, 13, 14, 15	12, 13, 14, 15	12, 13, 14, 15	12, 13, 14, 15
GRP2	2,5,8,11	TOP	0	16, 17, 18, 19	16, 17, 18, 19	16, 17, 18, 19	16, 17, 18, 19
			1	20, 21, 22, 23	20, 21, 22, 23	20, 21, 22, 23	20, 21, 22, 23
GRP3		BOT	1	24, 25, 26, 27	24, 25, 26, 27	24, 25, 26, 27	24, 25, 26, 27
			0	28, 29, 30, 31	28, 29, 30, 31	28, 29, 30, 31	28, 29, 30, 31
GRP4	3,6,9,12	TOP	0	32, 33, 34, 35			
			1	36, 37, 38, 39			
GRP5		BOT	1	40, 41, 41, 43			
			0	44, 45, 46, 47			

When the SMD works in 32 channel mode, only the top portion of the data are read out. Each readout contains $32 \times 4 = 128$ words (11 bits/word). While in the 48 channel mode, Only the data for TS = 0 portion are readout. Each readout contains 48 words.

SMD addressing scheme:

The addressing of SMD board is controlled by the SMC board. To reduce noise during the operation, gray code is used as addressing sequence for the normal readout. From the SMC board, address lines TS0, TS1, GRPSEL0 to GRPSEL3 are sent to the SMD. Decoding is done in a PLD called SMDTM on the SMD.

- The TS inputs are decoded in SMDTM from gray coded input sequence of TSA0 and TSA1 to regular ordered output sequence of TSB0 and TSB1 and sent to SMQIE chips.
- The GRPSEL0 to GRPSEL3 are decoded to the enable lines GRP0 to GRP5 and the channel selection signal CHSEL.

The following tables show the detail of the coding sequence of TS and GRPSEL signals.

INPUT		Decimal	OUTPUT		Decimal
TSA0	TSA1		TSB0	TSB1	
0	0	0	0	0	0
0	1	2	1	0	1
1	1	3	0	1	2
1	0	1	1	1	3

GRPSEL				Dec	Q. set	Enable line	SQD	TOP /BOT	CHSEL
0	1	2	3						
0	0	0	0	0	0	GRP0	1,4,7,11	TOP	0
1	0	0	0	1	1	GRP0		TOP	1
1	0	1	0	5	2	GRP1		BOT	1
0	0	1	0	4	3	GRP1		BOT	0
0	1	1	0	6	4	GRP2	2,5,8,11	TOP	0
1	1	1	0	7	5	GRP2		TOP	1
1	1	0	0	3	6	GRP3		BOT	1
0	1	0	0	2	7	GRP3		BOT	0
0	1	0	1	10	8	GRP4	3,6,9,12	TOP	0
1	1	0	1	11	9	GRP4		TOP	1
1	0	0	1	9	10	GRP5		BOT	1
0	0	0	1	8	11	GRP5		BOT	0

Conclusion:

As a conclusion, we will try to describe the channel number as a linear combination of several parameters. The formula may be found useful during programming of either test or analysis software.

We first define several numbers:

- The “quad set” number N_{QS} runs from 0 to 11. The first channel of a “quad set” N_{QS} is $4 \times N_{QS}$.
- The channel offset in a “quad set”, N_1 represents the N_1 -th channel in a “quad set”. It has a value of 0, 1, 2 or 3.

Therefore, the channel number $N = 4 \times N_{QS} + N_1$.