

The Shower Maximum Front End Electronics for the CDF Upgrade

A. Byon-Wagner, K. Byrum, J. W. Dawson, *Member, IEEE*, G. Drake, *Member, IEEE*,
C. Drennan, G. W. Foster, W. N. Haberichter, J. Hoff, S. Kuhlmann,
M. A. Lindgren, L. J. Nodulman, J. Proudfoot, J. L. Schlereth, and J. Y. Wu-

Abstract - The CDF Shower Max Electronics is part of the upgraded data acquisition system for the CDF experiment at Fermilab. The system services five detector subsystems of the calorimeter, and accommodates the different properties and data processing requirements imposed by each of them. The electronics is built around a custom integrated circuit called the SMQIE, which produces floating-point data with no dead-time using a 7.6 MHz clock. The components of the system are described, along with the principles of operation for performing data acquisition, calibration, and diagnostics.

I. INTRODUCTION

The Shower Max Front End Electronics is used by five detector subsystems in the upgraded CDF calorimeter [1]. Three detector subsystems are part of the Central Barrel. They are: the Central Electromagnetic Strip Chamber (CES), which is used to measure the position of electromagnetic showers in the central region of the detector; the Central Preradiator (CPR), which is used in conjunction with the CES to distinguish photons from low energy electrons; and the Central Crack Chamber (CCR), which is used to detect particles that might otherwise be lost in the cracks between wedges. The other two detector subsystems are part of the Forward Calorimeters (endplugs.) They are: the Plug Shower Maximum Detector (PES), which is used to measure the position of electromagnetic showers in the plug region; and the Plug Preradiator (PPR), which is used to separate electrons from photons. The three detectors in the Central Barrel use wire chamber technology, while the two detectors in the Plug use 16-channel multi-anode phototubes (MAPMT) with scintillating fibers. A summary of the properties of the detectors is given in Table 1. Despite the differences in the detectors, a goal in the design of the read-out system for the shower max detectors was to have the instrumentation be as

similar as possible for the five types of detectors. Most of the differences are handled by circuitry on the front end.

| <u>Property</u> | <u>Central</u> | <u>Plug</u> |
|-------------------------------|-----------------------------------|-----------------------|
| Detector Type | Proportional Chamber | 16 Ch Multi-Anode PMT |
| Detector Gain | ~1E3 | ~1E5 |
| Least Count Resolution | 3.3 fC (wires) 1.6 fC (strips) | 20 fC |
| Dynamic Range | 13 Bits | 13 Bits |
| Accuracy | 3% | 3% |
| Total # Channels | 11,232 | 6400 |
| Detector Capacitance | ~1 nF | ~100 pF |
| Noise Sensitivity | HIGH | LOW |
| Pulse Width | ~600 nS | ~70 nS |
| # Clocks / Pulse | 4 | 1 |
| Radioactive Source Monitoring | NO | YES |

Table 1. Summary of Detector Properties

II. DESCRIPTION OF SYSTEM COMPONENTS

The Shower Max Electronics is part of the data acquisition (DAQ) system for the CDF calorimeter. This system uses VIPA as the standard packaging for the front-end instrumentation [2]. The VIPA crates are mounted on the main detector. They interface to the trigger and data acquisition system as described in [1].

There are two primary parts to the Shower Max Electronics, as shown in Fig. 1. The analog processing circuitry is housed in crates called Shower Max Digitizer Crates (SMD Crates).

Manuscript received November 25, 2001. This work is sponsored by the U.S. Department of Energy under contract No, DE-AC02-76CH03000.

A. Byon Wagner, C. Drennan, G. W. Foster, J. Hoff, and J. Y. Wu are with Fermi National Accelerator Laboratory, Batavia, IL 60510 USA.

K. Byrum, J. W. Dawson, G. Drake, W. N. Haberichter, S. Kuhlmann, L. J. Nodulman, J. Proudfoot, and J. L. Schlereth are with Argonne National Laboratory, Argonne, IL 60439 USA.

M. A. Lindgren is with UCLA, Los Angeles, CA.

The operations performed by circuitry in the crate include the integration of the current pulses, digitization, and temporary storage of the data pending a trigger decision. The crates are located close to the shower max detectors, on the wedges of the Central Barrel and on the phototube enclosures of the endplugs. The close proximity of the SMD Crates to the detectors helps keep the signal cables short to reduce noise pickup.

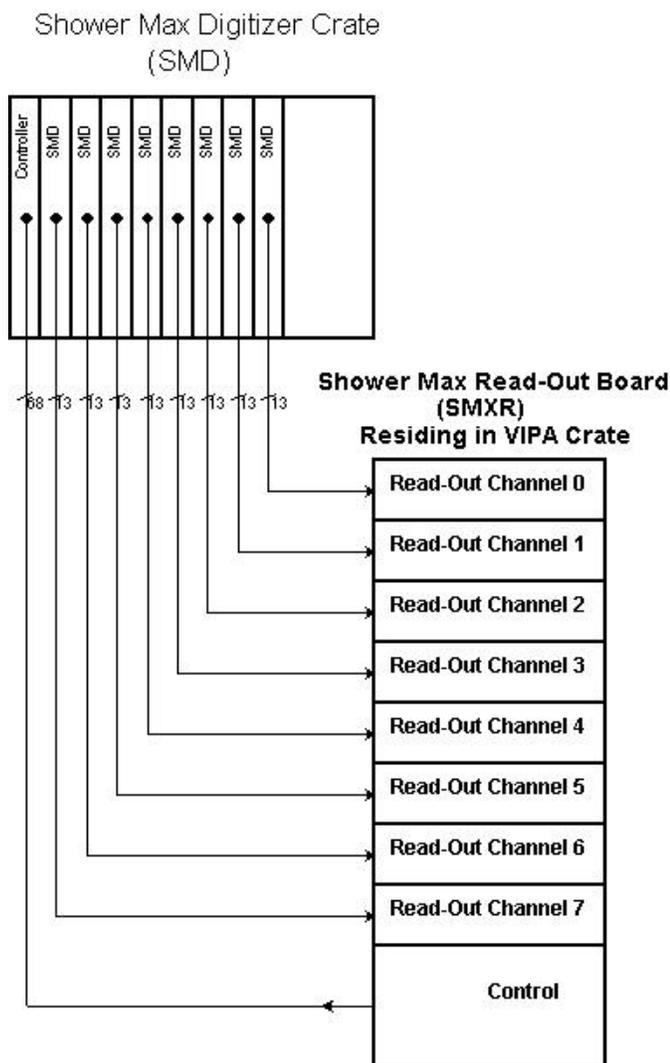


Fig. 1. Block Diagram of Readout System

Data is acquired and stored in the SMD Crates, and is held pending a Level 1 (L1) Trigger Decision. If the event is accepted, a Level 1 Accept (L1A) is issued by the Trigger System. This initiates a readout cycle, and causes digitized data to be sent from the boards in the SMD Crates to read-out boards in the VIPA Crates, which can be located some distance away. The VME computer that resides in each VIPA crate controls the collection of data from all the modules in the

crate. The data is then sent to the DAQ system for further processing. This arrangement reduces the number of expensive processors needed by the system, since the processor resources are shared by several front end subsystems. It also helps to reduce noise pickup by the detector from asynchronous digital activity, since the processors are kept off the detector.

The heart of the system is a custom integrated circuit called the SMQIE (Shower Max Charge (Q) Integrator and Encoder) [3]. It is a member of the QIE family of custom integrated circuits developed at Fermilab [4]. A version has also been designed for the calorimeter phototubes of CDF. The SMQIE is similar to these devices, but has additional on-board features. This device performs the entire analog signal processing for a detector channel. It contains a dead-timeless gated integrator with a 5-bit on-board flash ADC (FADC). It also contains a pipeline for storing events pending a Level 1 Trigger Decision, and four buffers for the temporary storage of selected data from the pipeline pending readout. The SMQIE chip contains two such circuits, and services two detector channels. The SMQIE is fabricated in a 1.2 μm , double-metal, double-poly process, and employs both CMOS and bipolar transistors.

The SMQIEs reside on daughter boards called SQUIDs (Shower Max QIE Ultracompact Integrated Daughter). The SQUID has a format that resembles a computer memory SIMM. Each SQUID contains two SMQIEs, so that each SQUID services four detector channels. In addition, the SQUIDs contain circuitry for measuring the average current from the MAPMTs, during detector calibration by a radioactive source. They also contain additional calibration circuitry, which injects precision DC current into the front-end electronics. A picture of both sides of a SQUID with SMQIE chips mounted is shown in Fig. 2.

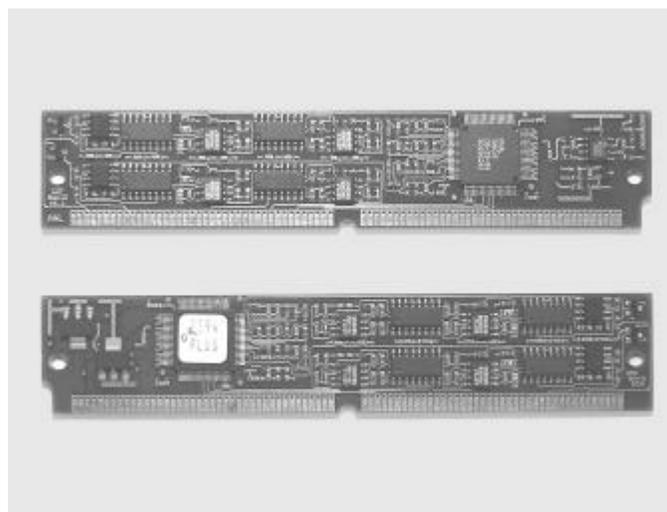


Fig. 2. Front and Back Views of a SQUID with Mounted SMQIEs

The SQUIDs reside on modules called SMD (Shower Max Digitizer) boards. The SMDs can hold up to 12 SQUIDs. In the case of the CES, CPR, and CCR, the SMD boards are configured with 8 SQUIDs, and service 32 detector channels each. In the case of the PES and PPR, the SMD boards are configured with 12 SQUIDs, and service 48 detector channels. A picture of the SMD Module is shown in Fig. 3.



Fig. 3. SMD Board with 12 SQUIDs

Preamps are used for the detector components in the Central Detector. These are current amplifiers. They receive the current pulses from the detector, amplify the signal, and then send them to the SMQIEs. The preamps have a differential input, and therefore can service both the cathodes (positive current) and the anodes (negative current) of the CES wire chamber. The gain is configured for each detector component. The preamps are mounted on Auxiliary (AUX) Boards, which plug into the back of the SMD crate. See Fig. 4.

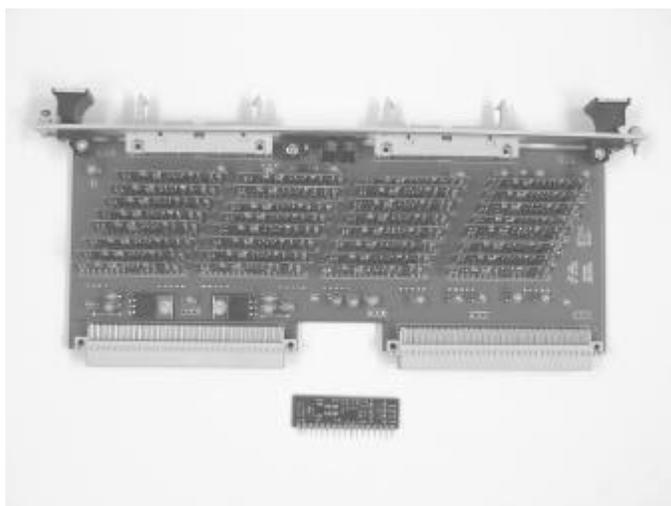


Fig. 4. Preamps Mounted on the AUX Card

The readout board that resides in the VIPA crate is called the SMXR (Shower Max Readout) Module. It is a 9U x 400 mm module that conforms to the VIPA standards. It acts as a data funnel, collecting data for an event from up to eight SMD boards for further processing. The data is sent from the SMD boards on a parallel cable using a 33 nS clock. It is received and processed in the SMXR, and then put into holding buffers where it can be accessed by the VME computer that resides in each VIPA crate. In addition, the SMXR has circuitry that can send data to the Level 2 Trigger System so that, in the case of the CES, information from the anodes can be used in the Level 2 Trigger Decision. It contains twelve Field-Programmable Gate Arrays (FPGAs), in which much of the logic is configured. A picture of the SMXR is shown in Fig. 5.

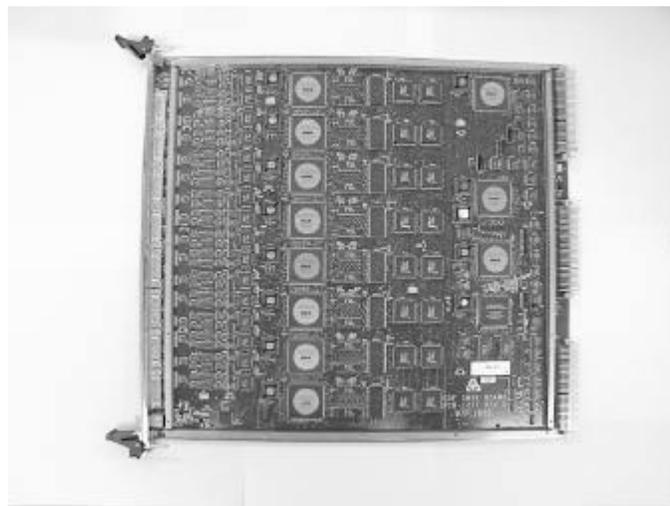


Fig. 5. The SMXR Readout Board

All activity in the SMD crate is controlled by a board in the crate called the SMC (Shower Max Controller.) The SMC in turn is controlled by the SMXR using a custom communication protocol. To initiate the acquisition of event data, the DAQ system sends signals to the VIPA crates, which are received by the SMXR. In turn, the SMXR sends signals to the SMC, which activates a sequencer on the SMC. The sequencing operation causes data to be sent from the SMD boards to the SMXR. The SMC also has a precision DAC, which is used by the calibration circuitry on the SQUIDs.

III. PRINCIPLES OF OPERATION

The SMQIEs receive and process current pulses from the detector using a gated integrator that operates with a 132 nS clock period. The gated integrator is implemented using circuitry called a "current splitter." The configuration uses 128 identical NPN transistors, as shown in Fig. 6. The emitters of all transistors are connected together at the input node, which is also connected to a bias current source. Without any input current coming in from the detector, the bias current divides

itself evenly between the 128 transistors. The collectors are grouped together in binary fashion. The group designated as "I/2" in Fig. 6 has the collectors of 64 of the 128 transistors connected together. Thus, the current into these collectors is equivalent to 64/128 of the bias current, or I/2. This is called the I/2 Range. Similarly, the I/4 Range sources 1/4 of the bias current, the I/8 Range sources 1/8 of the bias current, etc. The last two ranges use a single transistor each. Both the I/128 Range and the I/256 Range source 1/128 of the bias current. The sum of the current fractions from all the ranges equals 1. The current from each group is integrated on separate capacitors to form a binary-weighted voltage for that range. All capacitors are identical except for the I/256 capacitor, which is twice the size, yielding the proper binary ratio of voltages compared with the I/128 voltage. If additional current is pulled from the input node of the current splitter, as would occur by the detector in response to an event, the signal current is split in the same way, adding additional voltage onto each integrating capacitor.

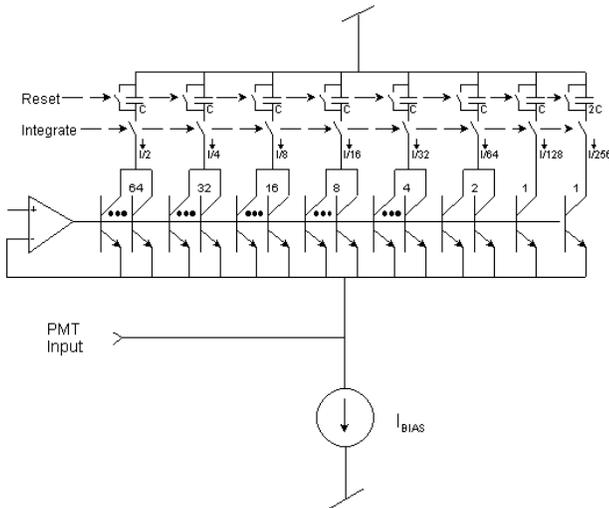


Fig. 6. Simplified Schematic of the SMQIE Current Splitter

The SMQIE has four phases of operation. The phase just described is the Integration Phase. At the end of this phase, all of the Sample-and-Hold switches are opened, and the resulting voltages are held on the integrating capacitors for further processing. The voltages from each capacitor are buffered and provided to a set of comparators inside the chip, which select one of the voltages for digitization. This is the Range Select Phase. The biasing is arranged such that one and only one of the ranges will be within the digitization range of the FADC. Once a range is selected, a 3-bit representation of the selected range is produced for output, called Range Bits. This phase takes one clock period.

Once a range has been selected for digitization, the Range Bits are stored in a register inside the chip, and the voltage on

the corresponding integration capacitor is switched to the input of an on-board, 5-bit FADC for digitization. Allowing for settling, the FADC is clocked at the end of this clock cycle. This is the Digitization Phase, and takes one clock period.

After the FADC has digitized, the Range Bits are appended to the FADC bits to form the floating-point data word, and the result is saved for further processing. The result is an 8-bit, floating-point word (3 Range Bits, 5 ADC bits.) It has an accuracy of 3%, and a dynamic range of 13 bits. The data is available for further processing on the clock cycle following the Digitization Phase.

The ideal transfer function for the SMQIE is shown in Fig. 7. The floating-point response must be converted to a linear form to be used for event reconstruction. This is described later.

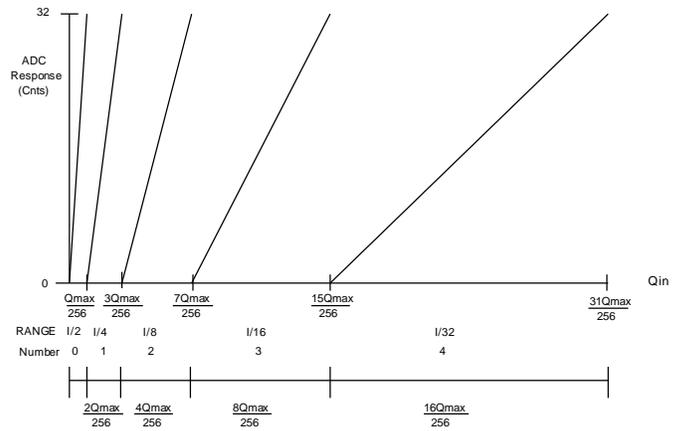


Fig. 7. Ideal SMQIE Transfer Function. (First 5 Ranges Shown.)

After the voltage on the selected integrating capacitor has been digitized, the integrating capacitors on all ranges are reset to prepare them for the next integration cycle. This is accomplished by briefly closing a switch around the integrating capacitor. This is the Reset Phase, and takes one clock cycle.

Note that after the Integration Phase, it takes three additional clock cycles to process the signal acquired on the integration capacitors and prepare for the next integration cycle. Without additional circuitry, the device would be dead 75% of the time. To accomplish dead-timeless operation, there are actually four sets of circuitry on each range. Each capacitor on a range is part of an overall phase of operation for the device. While one set of capacitors (one from each range) is integrating, another set is being selected for range, another set is being digitized, and the other set is being reset. The phase of operation changes with each clock cycle in round-robin fashion. In order to keep track of second order effects, a two-bit identifier is appended to each data word, called the

CAPID Bits. These bits identify the set of capacitors that were used to acquire and process a particular data word. This circuitry effectively pipelines the device, and produces dead-timeless operation. A data word is produced on every clock cycle.

After the SMQIE data word is formed, it is written into a memory inside the chip called the Level 1 Pipeline, which is 40 stages deep. The data is stored here while the Level 1 trigger decision is made using information from other parts of the CDF detector. The pipeline is configured as a shift register, where the data is moved along from stage to stage with each clock cycle. Once data is put into the Level 1 Pipeline, each data word is called a "timeslice," since the clocking is continuous and each word represents the response from the gated integrator over one clock period.

When an event is accepted by the Level 1 Trigger System, a Level 1 Accept (L1A) signal is sent to all front end systems. In the case of the shower max system, the L1A is received in the VIPA crate, sent onto the VIPA backplane, and is received by the SMXR. The SMXR in turn promptly sends the L1A to the SMC on the control link. The SMC sends the L1A onto the SMD Crate backplane, where it is received by all SMD modules in the crate, and fanned out to all SQUIDS. The timing of the system is such that the L1A is received by the SMQIE on precisely the clock cycle when the data of interest is at the end of the Level 1 Pipeline. If the data is to be captured, this must occur on the 42nd clock after the analog signal first appears at the SMQIE (40 pipeline stages, plus the Range Select Phase and the Digitization Phase.)

The Level 2 (L2) Trigger of the CDF Trigger System can process up to four events at a time. Events are held temporarily throughout the DAQ system in local memories called L2 Buffers. The Trigger System keeps track of which buffers are available for use. An L1A is issued only when there is an L2 buffer available. When the Trigger System issues an L1A, it also sends along a 2-bit identifier called the Level 2 Buffer Number, indicating which buffer that event is to be associated with. The SMXR sends the L2 Buffer Number to the SMD Crate, which in turn is sent to the SMQIEs. Inside the SMQIE, there are four holding registers called Level 1.5 Buffers, which correspond to the four Level 2 Buffers. Data is written into the selected buffer when the L1A is received. In order to accommodate reading out the slower detectors having charge signals that span over several clock cycles, the SMQIE was designed to save the last 4 timeslices at the end of the pipeline when an L1A is received. These timeslices can be added together later to obtain a better measure of the signal for the slow signals. After the data is stored in one of the L1.5 Buffers, it can be read out at a later time. The data that was written into the L1.5 Buffer stays there until it is overwritten by a new L1A with that buffer number.

When the L1A and L2 Buffer Number are received by the SMXR, in addition to sending them to the SMQIEs, it also puts them into a processing queue. The SMXR acts on each event in turn. To begin a data transmission cycle, the SMXR send a Data Transmission Request (DTR) to the SMC, along with the requested buffer number to read. When the SMC receives the DTR, it sends a pre-defined sequence of control signals across the backplane of the SMD Crate. These signals cause data to be accessed from the L1.5 Buffers in the SMQIEs, and sent from the SMD boards to the SMXR. There is one data bus on each SMD, so that only one channel on each SMD can be active at a time. The SMC controls the selection of the channel, the buffer number, and the timeslice number. For the PES and PPR, only one timeslice is needed, since the charge signal is completely acquired in one clock cycle. For the slower detectors of the Central Barrel, four timeslices are read. The sequencer on the SMC is implemented in programmable logic, and has a different sequence of operations for each type of detector.

All SMD modules in an SMD Crate receive and process the control signals from the SMC at the same time. As data words are accessed from the L1.5 Buffers in the SMQIEs, the SMDs send the data to the SMXR. The data is sent to the SMXR on a 33 nS clock cycle. For the PES and PPR, the number of words sent is 48 (48 channels, 1 timeslice/channel.) For the CES, CPR, and CCR, the number of words sent is 128 (32 channels, 4 timeslices/channel.)

When data is received by the SMXR, it is written into an input FIFO (First In-First Out memory,) one for each data stream. Each input channel processes data independently of the others. Control logic on the SMXR polls each FIFO looking for a header bit, which is sent by the SMD on the first data word in a transmission cycle. When the header bit is encountered, the SMXR reads data words from the input FIFO, and processes them through a Look-Up Table (LUT). The LUT is used to transform floating-point QIE data words into 13-bit linear words, a process called "linearization." The QIE data words serve as addresses for the LUT, the contents of which contain the linearized values. The values of the LUT are obtained using a calibration procedure that is done beforehand.

In the case of the detectors in the Plugs, the data word is written to the selected L2 Buffer on the SMXR. In the case of the detectors from the Central Barrel, the linearized data corresponding to the four timeslices for each channel are added together to reconstruct the charge pulse. The data is then written to the L2 Buffer. The SMXR processes all the data in the FIFO until the FIFO is empty. It then checks a word count, and compares it with the number of words expected. An error is generated if the numbers do not match.

When the data processing is completed, the SMXR goes to the next event in the queue. The data processing continues in this fashion as long as there are entries in the queue. When the processing for a particular L2 Buffer is completed, the data is accessed by the computer in the VIPA crate, and it is sent to the higher levels of the DAQ system.

IV. PERFORMANCE

The production and installation of the system were completed in March 2001. In all, there are 18,192 channels instrumented on the detector. The physics run began in June 2001. There have now been many months of experience with the system, and the experiment is currently running with proton-antiproton collisions.

Before a physics run begins, the LUTs must be loaded. This is accomplished by measuring the pedestals, and using the DC current injection circuitry on the SQUIDS. The calibration circuitry is enabled, and the DAC on the SMC is stepped through a range of values. The response from all of the SMQIE channels is measured, and averages calculated for each DAC setting. The response of a typical PES channel from DC current injection is shown in Figure 8. All 8 ranges are represented, although the first 3 ranges appear merged together on this scale.

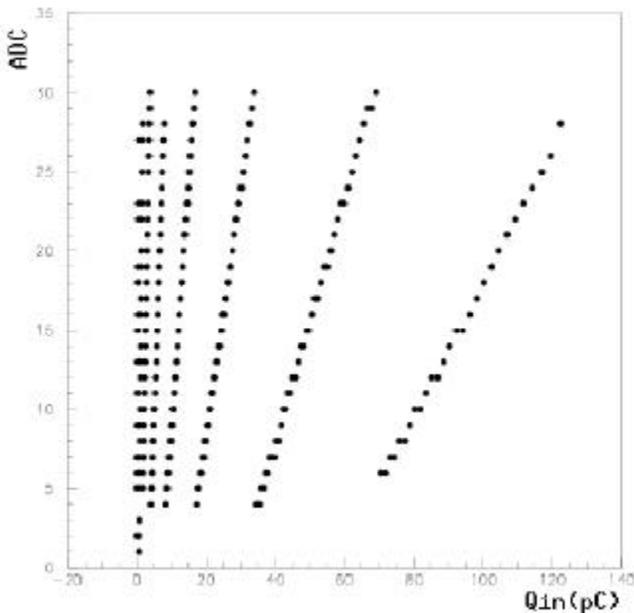


Fig. 8. SMQIE Response to DC Current Injection

After the data is acquired, the slopes and offset of all ranges are calculated, for each capacitor ID on every channel. The calculations are done in the processor that resides in each

VIPA crate, taking advantage of the high degree of parallel processing available in the system. Once the pedestals, and slopes and offsets of each of the SMQIE ranges are measured, they are used to calculate the corresponding linear values associated with every possible SMQIE code. The values are then downloaded into LUTs on the SMXR. The address for a particular LUT location is formed from the channel number, capacitor ID, range value, and ADC value. The value written to that memory location is the calculated linearized value. The pedestals and calibration constants are also written into to a database where they are stored and used for monitoring performance and stability.

The sensitivity of the system is determined by noise, both intrinsic and from the environment. The channels in the endplugs have the best noise performance, since the photomultiplier tubes have low intrinsic noise and are relatively immune to environmental noise. The distribution of RMS values for the PES is shown in Figure 9. Typical RMS noise values are less than 0.5 SMQIE counts, where each count corresponds to 20 fC of charge.

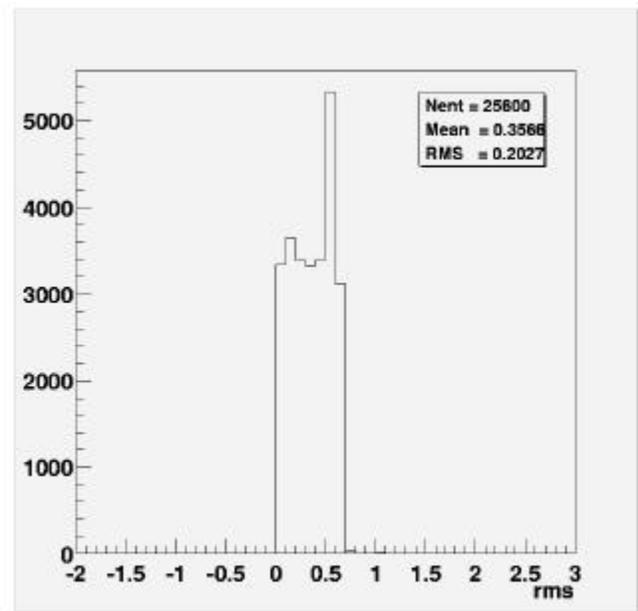


Fig. 9. Distribution of RMS Values for All PES Channels (Each Channel has 4 Entries, One for Each Capacitor ID)

The noise performance of the detector and electronics of the Central Barrel is dominated by environmental noise. Much of the noise is coherent. The distributions of pedestal RMS values for the anodes (wires) and cathodes (strips) of the CES are shown in Fig. 10. The measurement shown is obtained from a single 132 nS gate. When four timeslices are added together, the equivalent noise is worse. If there were no coherent noise component, the RMS from adding four

timeslices would be a factor of two larger. Because there is a large coherent noise component, the RMS values from adding four timeslices are approximately a factor of 3 larger than that of a single timeslice. Noise abatement techniques were implemented in an attempt to reduce the noise. The preamp has a differential input with ~ 40 db of common mode rejection. The signal cables are shielded with a commercial foil shield. Additional local grounding was added to the chambers by grounding the braid of the high voltage cables. These steps helped, but ultimately the noise was dominated by noise pick-up within the chamber from the environment. Because the noise is coherent, an algorithm was developed in which the coherent component of the noise is measured and subtracted from the data. Using this technique and the other noise reduction steps, acceptable noise performance was achieved. This was important for accurately measuring the position of soft electromagnetic showers, as well as soft electron tagging and optimized jet energy reconstruction, which all use the strips to characterize the electromagnetic energy in a calorimeter tower.

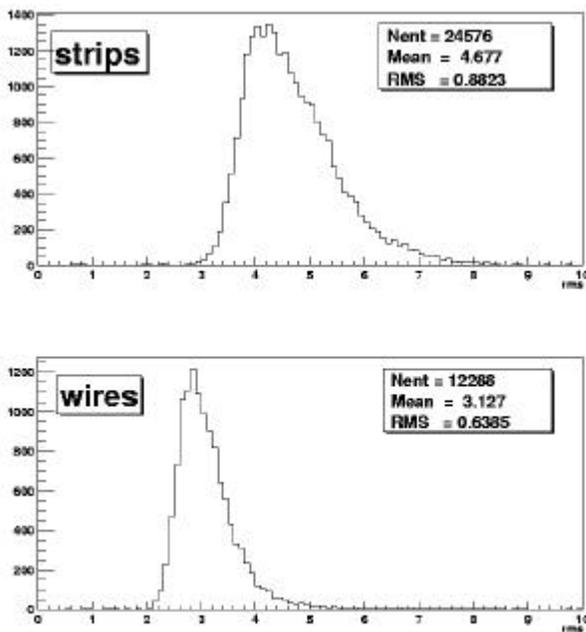


Fig. 10. Distribution of RMS Values for All CES Channels (Each Channel has 4 Entries, One for Each Capacitor ID)

The CDF detector is a complicated apparatus consisting of a large number of separate detectors. The data from the different detector components must be combined for every interaction to form complete, single “events”. Each detector element in the system has a different signal propagation time and a different processing time. For the results to be useful, each detector subsystem must have the timing set properly. This includes adjusting the relative phase of the clock used for

signal acquisition, and adjusting the timing of when the data of interest is captured and stored in response to a L1A.

For the shower max detectors, the timing of both the L1A and the SMQIE clock can be varied by using programmable delays built into the system. The L1A can be moved in whole number increments of the 132 nS clock to capture the data of interest associated with a particular L1A. The determination of the correct setting for the L1A was accomplished by reading out the detector and varying the timing of the L1A until the signal appeared in time with the rest of the detectors. For this procedure, the detector was operated in data acquisition mode with four L1A's generated on consecutive clock cycles. This provided a method for identifying how the charge signals were processed in time. In the detectors of the Central Barrel where the detector signal is distributed across multiple timeslices, the summing algorithm on the SMXR had to be turned off so that only a single timeslice was read. In the plug detectors, no such algorithm is used since most of the signal appears within one timeslice.

Once the L1A timing was set, the timing of the integration gate was adjusted to position the leading edge of the signal as close as possible to the beginning of the 132ns gate. The SMQIE clock can be adjusted in ~ 2 nS steps fractional units of the 132 nS clock cycle to optimize the integration gate for the charge signal coming from the detectors. The method that was used to adjust the L1A timing was used again, to observe the response in each individual timeslice. A representative result from the endplug electronics is shown in Fig. 11. In the plot, TS0 is the fraction of charge in the first timeslice, and TS1 is the fraction of charge in the second timeslice, as the phase of SMQIE clock is shifted in time.

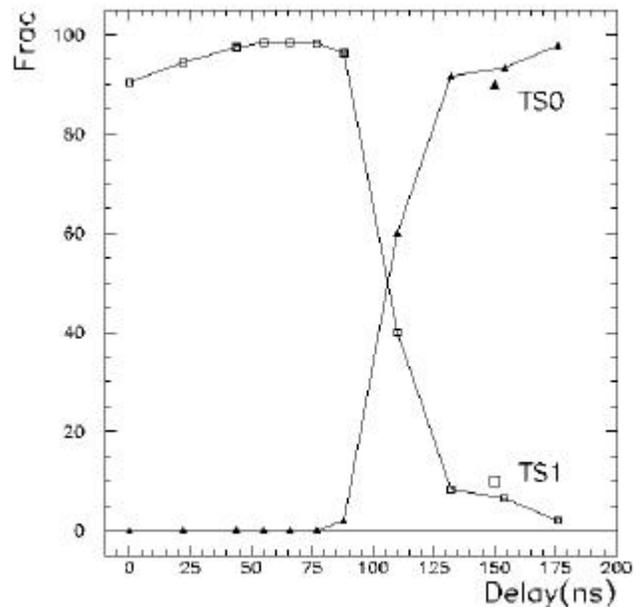


Fig. 11. Fractional Division of Charge as a Function of Phase Delay of SMQIE Clock for the Endplug Electronics

ACKNOWLEDGEMENT

The authors wish to thank the technical staff of the Fermilab Particle Physics Division for the support in building and producing the electronics of this system.

REFERENCES

- [1] The CDF Collaboration, "The CDF II Detector, Technical Design Report," FERMILAB-Pub-96/390-E, Chapters 8 and 9, November, 1996.
- [2] VITA Standards Organization, "VME64 Extensions for Physics/VME64xP," ANSI/VITA 23-1998.
- [3] J.Hoff, G. Drake, A. Byon Wagner, G. W. Foster, M. Lindgren, "SMQIE: A Charge Integrator and Encoder Chip for the CDF Run II Shower Max Detector," *IEEE Trans. on Nuclear Science*, vol. 47, pp. 834-838, June, 2000.
- [4] R.J.Yarema, G. W. Foster, J. Hoff, M. Sarraj, T. Zimmerman, "A Fast, Wide Range Charge Integrator and Encoder ASIC for Photomultiplier Tubes," *IEEE Trans. on Nuclear Science*, vol. 40, pp. 750-752, Aug., 1993.

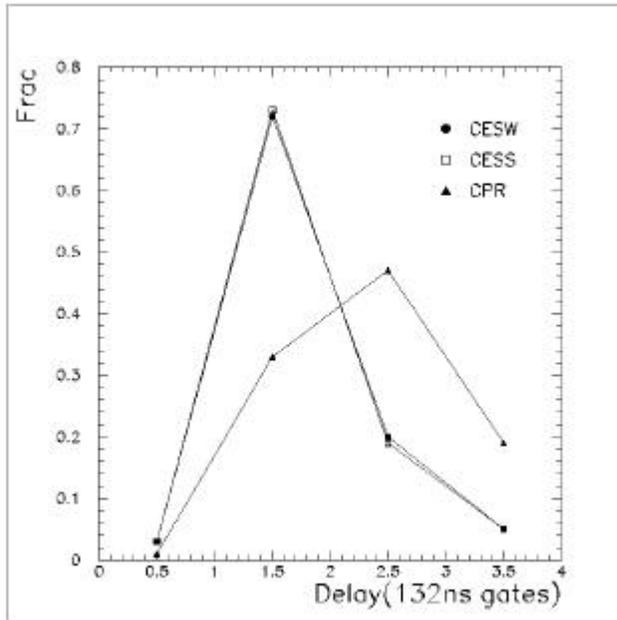


Fig. 12. Fractional Division of Charge as a Function of Timeslice for the CES and CPR Detectors of the Central Barrel

v. SUMMARY

The CDF Shower Max Electronics has been produced, installed, and commissioned. The system is now fully functional. The electronics is capable of operating in a high-rate environment, and meets the performance requirements needed for measuring interactions from high center of mass energy collisions. The use of a custom integrated circuit specifically designed for this application has made it possible to obtain high speed and high performance for this important detector subsystem. We look forward to a rich running period of the Fermilab Tevatron.